AI 046

S-DIAS Analog Input Module

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Translation from German

S-DIAS Analog Input Module AI 046

with 4 analog inputs ±11 V or ±1.1 V

The S-DIAS analog input module AI 046 has four analog inputs with two adjustable measurement ranges with ±11 V or ±1.1 V with an 18-bit resolution. The voltage supply for the analog inputs are monitored for under voltage. The analog inputs are galvanically separated from the S-DIAS bus.

Contents

1 Technical Data

1.1 Analog Input Specifications

Number of channels	4	
Measurement range [1]	-11 … +11 V	-1.1 … +1.1 V
Amplification	1	10
Measurement value	-110,000 ... +110,000 (Mode: 18-bit signed value range) -27,500 ... +27,500 (Mode: 16-bit signed value range)	
Galvanic isolation	500 V (maximum isolation voltage)	
Input type	difference input	
A/D converter	18-bit SAR with simultaneous scanning	
Measurement range resolution	18-bit	
	ca. 84 µV/LSB	ca. 8.4 µV/LSB
Scan rate per channel	≤ 10 µs (minimum S-DIAS cycle time: 100 µs)	
Data memory depth per channel	512 Dwords (32 bits) 1024 words (16 bits)	
Calculation basis for number of values per channel (n)	n = S-DIAS cycle time / scan rate	
Common mode range	±12 V	±6 V
Input resistance	typically 5 MΩ	
Cable break monitor	yes (10 MΩ between AI+ and +12 V, 10 MΩ between AI- and -12 V)	
Input filter hardware [2]	10 kHz, low pass 3rd order (differential mode) 100 kHz, low pass 1st order (common mode)	
Input filter software [3]	configurable	
Maximum allowable input voltage	±30 V	
Total measurement precision Measurement method: Mode 2, sampling rate 50 µs	±0.030 % (20-40 °C) ±0.045 % (0-55 °C)	±0.045 % (20-40 °C) ±0.060 % (0-55 °C)
Status display	green LED	

[1] If the upper or lower limit of a measurement range is exceeded, it will display a corresponding status bit.

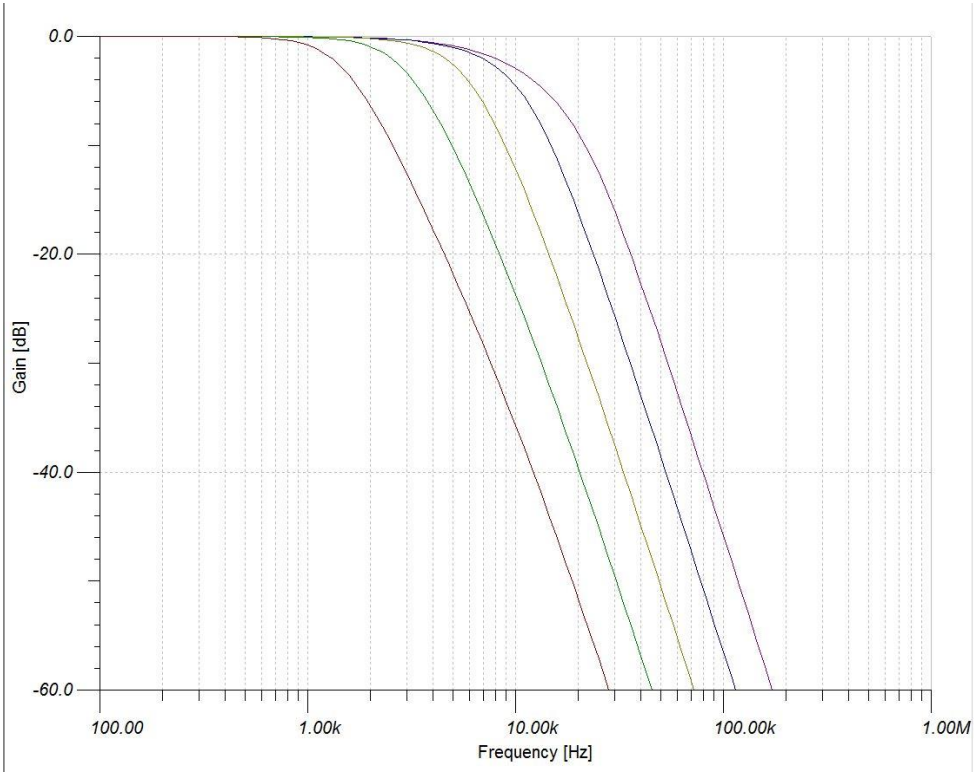
(2) The filter parameters (frequency and order) for differential mode are depending on the scan rate in mode 2. An overview can be found in the table below. The frequency responses are shown in the diagrams below.
(3) This is a 1st order IIR filter, which has an adjustable frequency and can also be deactivated. **Caution!** The SW filter does not replace the HW filter! The SW filter only functions correctly when the Nyquist-Shannon theorem is observed.

1.2 Measuring Modes

Scan rate (µs)	Mode 1 (1)	Mode 2 (2)
	hardware frequency limit in kHz	hardware frequency limit in kHz
10	10	10
20	10	10
25	10	10
50	10	8
100	10	5
200	10	3
250	10	3
500	10	1.5
1000	10	1.5

(1) with oversampling in FPGA
(2) with oversampling in ADC (the integrated HW filter in the ADC changes depending on the defined sampling rate)

Typical frequency curves for the frequency limits 1.5 kHz (brown), 3 kHz (green), 5 kHz (yellow), 8 kHz (black) and 10 kHz (purple).



1.3 Measurement Precision

Measurement range	-11 … +11 V	-1.1 … +1.1 V
Accuracy incl. calibration error and noise Mode 2, sampling rate 50 µs 25 °C	0.010 %	0.017 %
Temperature drift 20-40 °C 0-55 °C	 0.006 % 0.020 %	 0.008 % 0.025 %
Linearity	0.003 %	0.005 %
Crosstalk	0.003 %	0.003 %
Symmetry	0.009 %	0.010 %
Total error 20-40 °C 0-55 °C	 ±0.030 % (±3.3 mV) ±0.045 % (±5.0 mV)	 ±0.045 % (±0.50 mV) ±0.060 %(±0.66 mV)

Tolerances, which are caused by aging, are not taken into consideration. A calibration is necessary after 12 months at the latest.

1.4 Electrical Requirements

External voltage supply X5	18-30 V DC	
Current consumption X5 [1)]	maximum 650 mA (maximum 500 mA for all sensor supplies) typically 60 mA (electronics)	
Voltage supply from S-DIAS bus	+5 V	
Current consumption on the S-DIAS bus (+5 V supply)	0	0
Voltage supply from S-DIAS bus	+24 V	
Current consumption on the S-DIAS bus (+24 V supply)	typically 30 mA	maximum 35 mA

(1) The outgoing sensor supply for X1, X2, X3 and X4 are fed via X5. Using a PTC fuse, a common fuse is provided for the sensor supplies for a maximum of 500 mA

If this S-DIAS module is connected to an S-DIAS supply module with several S-DIAS modules, the total current of the modules used must be determined and checked.

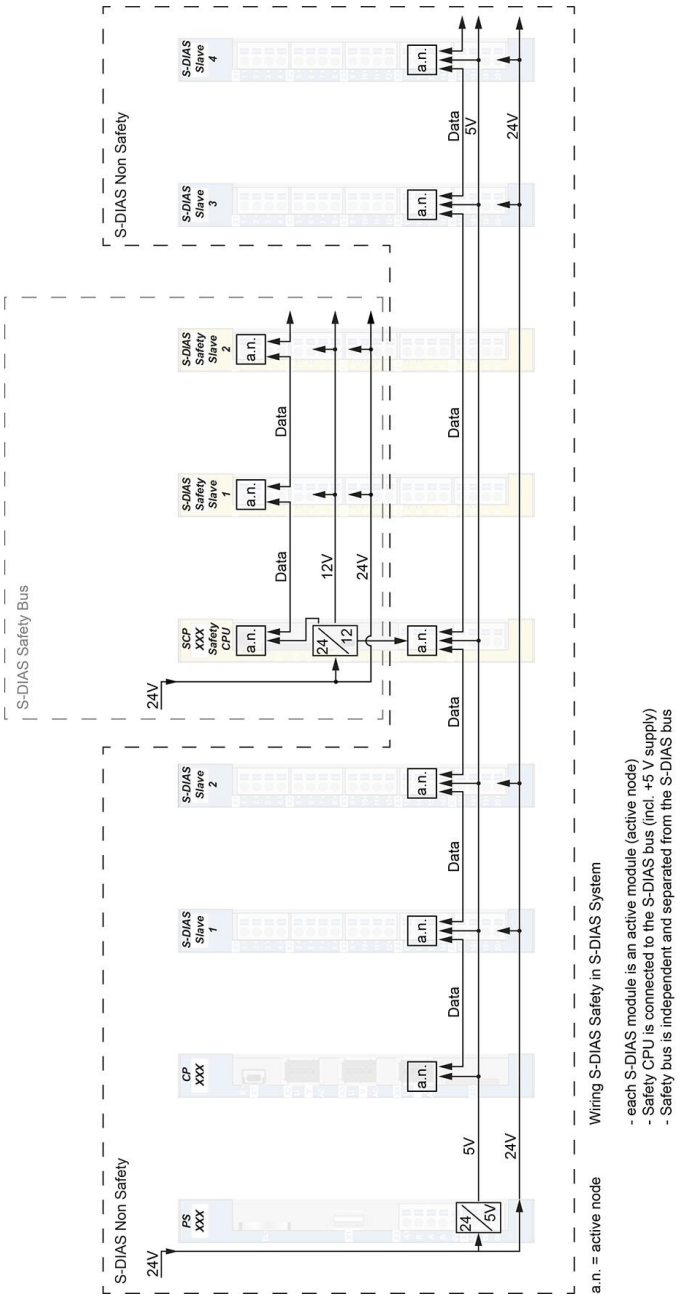
The total current of the +24 V supply cannot exceed 1.6 A!
The total current of the +5 V supply cannot exceed 1.6 A!

The specification for the current can be found in the module-specific technical documentation under "Electrical Requirements".

Si ce module S-DIAS est connecté à un module d'alimentation S-DIAS suivi de plusieurs modules S-DIAS, le courant total des modules utilisés doit être déterminé et vérifié.

Le courant total de l'alimentation +24 V ne peut pas dépasser 1,6 A!
Le courant total de l'alimentation +5 V ne peut pas dépasser 1,6 A!

Le cahier des charges pour le courant peut être trouvé dans la documentation spécifique au module sous "Spécifications électriques".


S-DIAS Non Safety
S-DIAS Safety Bus
S-DIAS Non Safety
24V
PS XXX
CP XXX
S-DIAS Slave 1
S-DIAS Slave 2
SCP XXX Safety CPU
S-DIAS Safety Slave 1
S-DIAS Safety Slave 2
S-DIAS Slave 3
S-DIAS Slave 4
a.n.
Data
5V
12V
24V
24/5V
24/12
a.n. = active node
Wiring S-DIAS Safety in S-DIAS System
- each S-DIAS module is an active module (active node)
- Safety CPU is connected to the S-DIAS bus (incl. +5 V supply)
- Safety bus is independent and separated from the S-DIAS bus

1.5 Voltage Monitor External +24 V Supply

Power supply +24 V	supply voltage > 18 V (DC OK-LED lights green)

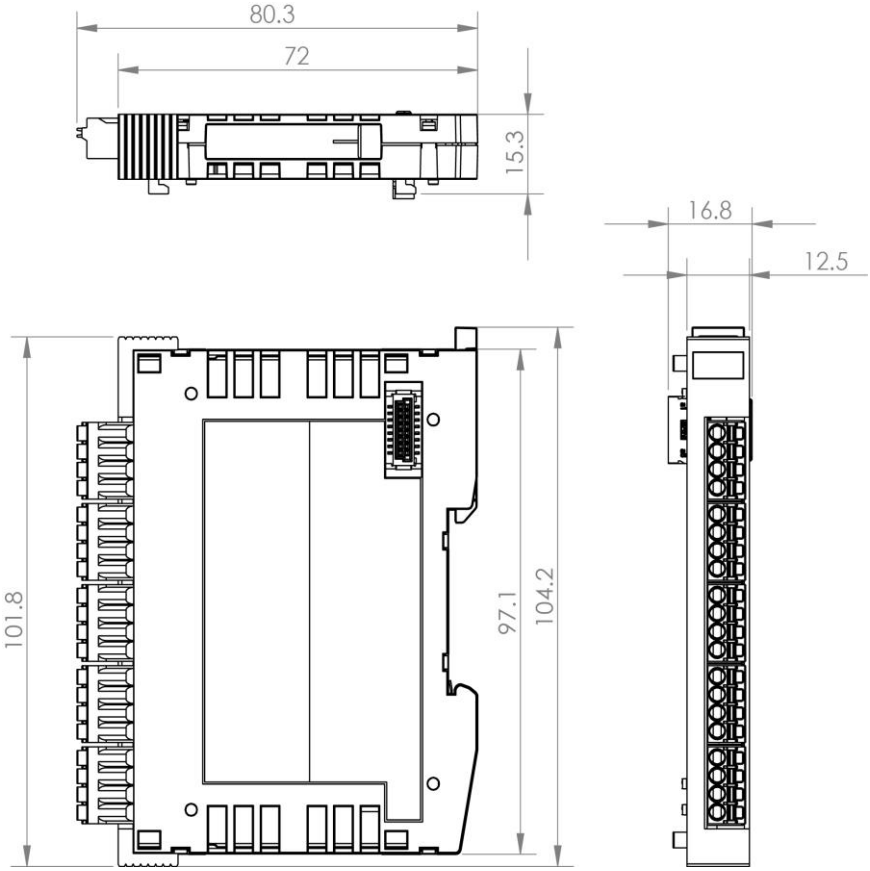
1.6 Miscellaneous

Article number	20-009-046
Hardware version	1.x
Standard	UL in preparation

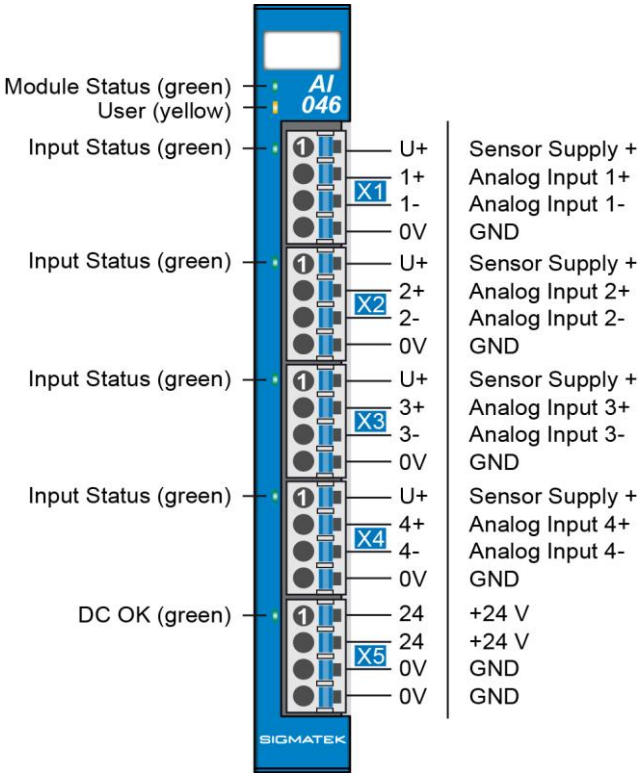
1.7 Environmental Conditions

Storage temperature	-20 ... +85 °C	
Environmental temperature	0 ... +55 °C	
Humidity	0-95 %, non-condensing	
Operating conditions	Pollution degree 2 altitude up to 2000 m	
EMC resistance	in accordance with EN 61000-6-2 (industrial area)	
EMC noise generation	in accordance with EN 61000-6-4 (industrial area)	
Vibration resistance	EN 60068-2-6	3.5 mm from 5-8.4 Hz 1 g from 8.4-150 Hz
Shock resistance	EN 60068-2-27	15 g
Protection type	EN 60529	IP20

2 Mechanical Dimensions



3 Connector Layout



The connections of the +24 V supply (X5: pin 1 and pin 2) or the GND supply (X5: pin 3 and pin 4) are internally bridged. To supply the module, only one connection to a +24 V pin (pin 1 or pin 2) and a GND pin (pin 3 or pin 4) is required. The bridged connections may be used for further looping of the +24 V supply and the GND supply. However, it must be taken into account that a total current of 6 A per connection is not exceeded by the forward looping!

3.1 Status LEDs

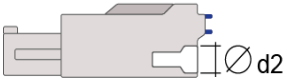
Module Status	green	ON	module active
		OFF	no supply available
		BLINKING (5 Hz)	no communication
User	yellow	ON	can be set from the application (e.g. the module LED can be set to blinking through the visualization so that the module is easily found in the control cabinet)
		OFF	
		BLINKING (2 Hz)	
		BLINKING (4 Hz)	
Input Status	green	ON	analog input active
		BLINKING (0.5 Hz)	analog input below measurement range
		BLINKING (4 Hz)	analog input above measurement range
		OFF	analog input inactive
		USER	LED can be optionally controlled via the application
DCOK	green	ON	+24 V supply for analog inputs available

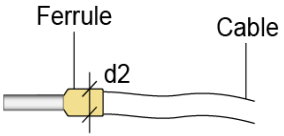
3.2 Applicable Connectors

Connectors:
X1-X5: Connectors with spring terminals (included in delivery)
The spring terminals are suitable connecting ultrasonically compacted (ultrasonically welded) strands.

Connections:

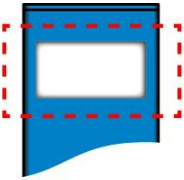
Stripping length/Sleeve length:	10 mm
Mating direction:	parallel to the conductor axis or circuit board
Conductor cross section rigid:	0.2-1.5 mm^2
Conductor cross section flexible:	0.2-1.5 mm^2
Conductor cross section ultrasonically compacted:	0.2-1.5 mm^2
Conductor cross section AWG/kcmil:	24-16
Conductor cross section flexible with ferrule without plastic sleeve:	0.25-1.5 mm^2
Conductor cross section flexible with ferrule with plastic sleeve:	0.25-0.75 mm^2 (reason for reduction d2 of the ferrule)





d2 = max. 2.8 mm

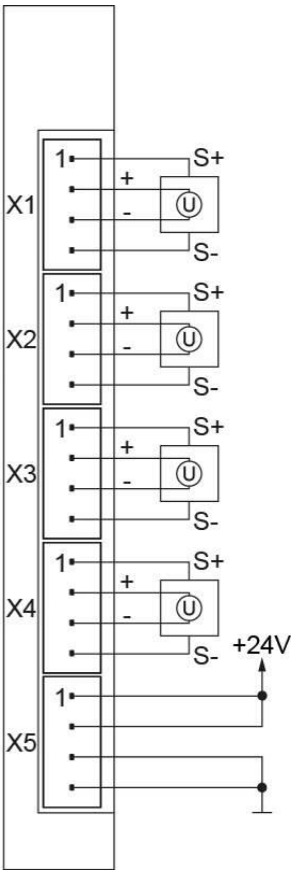
3.3 Label Field



Manufacturer	Weidmüller
Type	MF 10/5 CABUR MC NE WS
Weidmüller article number	1854510000
Compatible printer	Weidmüller
Type	Printjet Advanced 230V
Weidmüller article number	1324380000

4 Wiring

4.1 Wiring Example



NOTE

Unused inputs should be bridged between analog input + and analog input - using a short-circuit jumper. Open inputs have no functional effect on the module, but lead to higher current consumption in the external supply of the module.

4.2 Note

To ensure error-free operation, a careful wiring method must be followed:

- The 0 V connection of the supply voltage must be connected with the 0 V collection point over the shortest route possible.
- The DIN rail must have an adequate mass connection.
- The lines connected to the source of the analog components must be as short as possible and parallel wiring to digital signal lines must be avoided.
- The signal lines must be shielded.
- The shielding must be connected to a shielding bus.
- Protective circuits for all relays (RC networks or free-wheeling diodes)
- Correct wiring to mass

The ground bus should be connected to the control cabinet when possible!

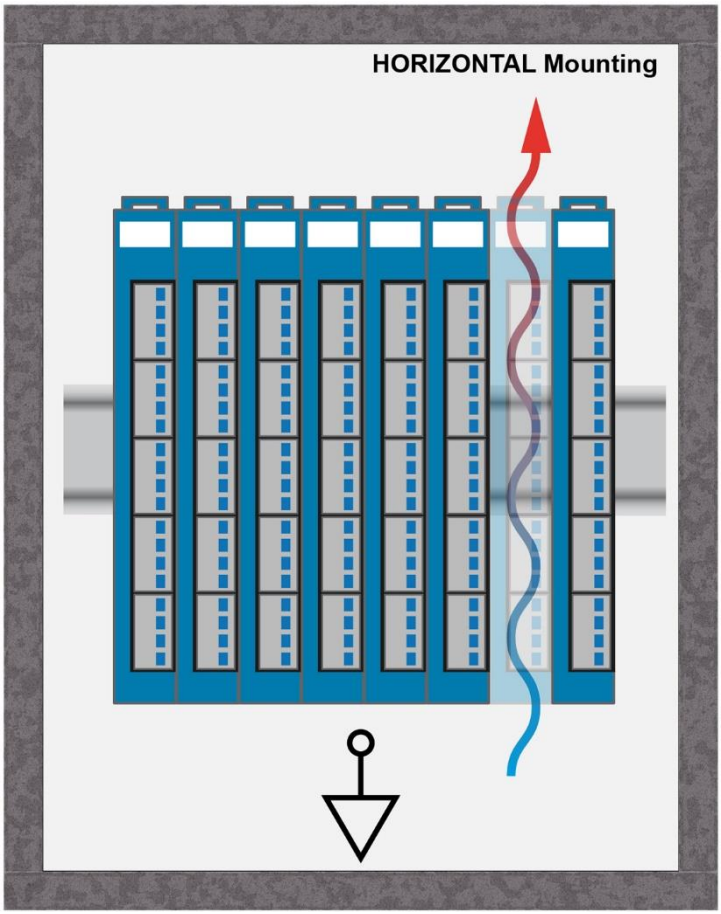
Si possible la terre doit être connectée à l'armoire de commande!

IMPORTANT:
The S-DIAS module CANNOT be connected/disconnected while voltage is applied!

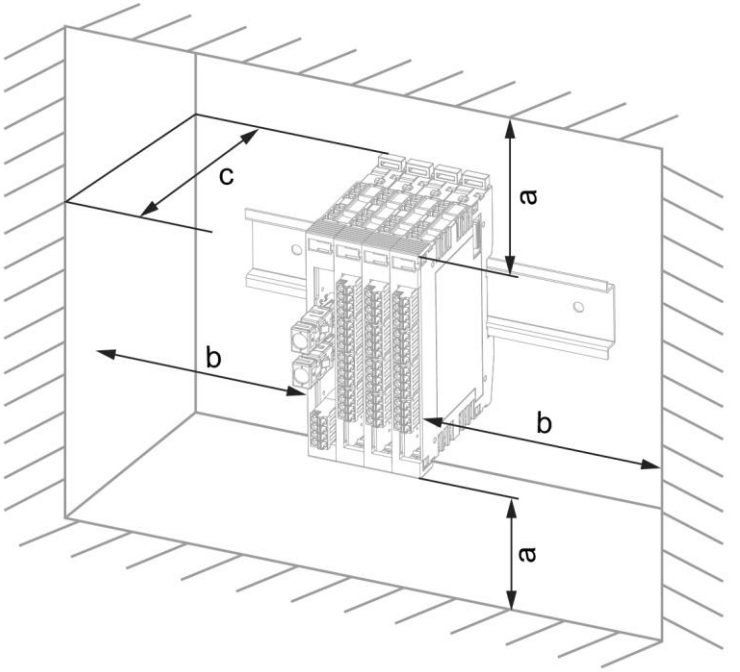
IMPORTANT:
Le module S-Dias NE PEUT PAS être inséré ou retiré sous tension.

5 Mounting

The S-DIAS modules are designed for installation into the control cabinet. To mount the modules a DIN-rail is required. The DIN rail must establish a conductive connection with the back wall of the control cabinet. The individual S-DIAS modules are mounted on the DIN rail as a block and secured with latches. The functional ground connection from the module to the DIN rail is made via the grounding clamp on the back of the S-DIAS modules. The modules must be mounted horizontally (module label up) with sufficient clearance between the ventilation slots of the S-DIAS module blocks and nearby components and/or the control cabinet wall. This is necessary for optimal cooling and air circulation, so that proper function up to the maximum operating temperature is ensured.



Recommended minimum distances of the S-DIAS modules to the surrounding components or control cabinet wall:



a	b	c
30 mm (1.18″)	**30 mm** (1.18″)	**100 mm** (3.94″)

a, b, c … distances in mm (inches)

6 Configuration

To start, once the module is powered, the FPGA located in the microcontroller (MicroBlaze) is in Rest mode. If the reset for the MicroBlaze is deactivated via the "SDO control register", the microcontroller begins its configuration phase. As soon as this is complete, bit 3 Operational in the "Error/Status register" is set.

When a change is made in the SDO area, the settings are first assumed when bit 6 in the "SDO control register" is set. For the duration of the configuration phase, bit 3 Operational is inactive.

The data memory or each channel is filled with a defined number of values. The number of values in the data memory results from the configured S-DIAS cycle time and the scan rate. The values are written to the data memory in 16-bit mode as Word or in 18-bit mode, as Dword. In 16-bit mode, the number of bytes to read is reduced and therewith, the load on the S-DIAS bus. 16-bit/18-bit mode is set in the "SDO control register".

The data memory of each channel is filled when the respective channel is activated via the "PDO control register".

Using an alternating buffer, data consistency is ensured. The data memory is filled during an S-DIAS cycle and released at the end of the cycle. The values are then valid in the subsequent S-DIAS cycle for the duration of an S-DIAS cycle.

When setting the scan rate, FPGA oversampling and ADC oversampling, the required conversion time of the ADC and the transfer rated via SPI must be taken into consideration. From the resulting number of conversions, an average value is generated that is then written to the data memory. The following settings for the scan rate and oversampling are recommended:

6.1 FPGA Oversampling

Scan Rate	FPGA Oversampling	ADC Oversampling	Values within an S-DIAS Bus Cycle with 1 ms	Hardware Frequency Limit [kHz]
10	0 (1x)	0 (1x)	100	10
20	1 (2x)	0 (1x)	50	10
25	1 (2x)	0 (1x)	40	10
50	2 (4x)	0 (1x)	20	10
100	3 (8x)	0 (1x)	10	10
200	4 (16x)	0 (1x)	5	10
250	4 (16x)	0 (1x)	4	10
500	5 (32x)	0 (1x)	2	10
1000	6 (64x)	0 (1x)	1	10

6.2 ADC Oversampling

Scan Rate	FPGA Oversampling	ADC Oversampling	Values within an S-DIAS Bus Cycle with 1 ms	Hardware Frequency Limit [kHz]
10	0 (1x)	0 (1x)	100	22.0
20	0 (1x)	1 (2x)	50	22.0
25	0 (1x)	2 (4x)	40	18.5
50	0 (1x)	3 (8x)	20	11.9
100	0 (1x)	4 (16x)	10	6.0
200	0 (1x)	5 (32x)	5	3.0
250	0 (1x)	5 (32x)	4	3.0
500	0 (1x)	6 (64x)	2	1.5
1000	1 (2x)	6 (64x)	1	1.5

7 Addressing

Address (hex)	Size (bytes)	Access Type	Description	Reset value
0000	**532**	**r**	**PDO Read**	
0000	128	r16/32	Data memory channel 1 (16/32 bits) Data memory => if more than 128 bytes of data are available, the data is provided when rereading the next data. Unread data are no longer available in the next cycle. 16/32 bit => depending on the setting in the "control register", bit 0 of address 0x0229, the individual data sets are provided as Word or Dword (resolution is lower when read as word). All values are signed.	0000
0080	128	r16/32	Data memory channel 2 (16/32 bits)	0000
0100	128	r16/32	Data memory channel 3 (16/32 bits)	0000
0180	128	r16/32	Data memory channel 4 (16/32 bits)	0000
0200	2	r16	Data memory status register (Data memory is set to full when the current memory for the respective channel is full) Bit 0: Memory full channel 1 Bit 1: Memory full channel 2 Bit 2: Memory full channel 3 Bit 3: Memory full channel 4 (Data memory is set to empty when the current memory for the respective channel is empty) Bit 4: Memory empty channel 1 Bit 5: Memory empty channel 2 Bit 6: Memory empty channel 3 Bit 7: Memory empty channel 4 (If a memory area is read, although no data available, "Read on empty memory" is set) Bit 8: Read on empty memory channel 1 Bit 9: Read on empty memory channel 2 Bit 10: Read on empty memory channel 3 Bit 11: Read on empty memory channel 4 Bit 12: DC 24 V not ok latched Bit 13: DC 24 V ok Bit 14-15: Reserved	00
0202	1	r	Hardware status latch register (bytes are reset after reading) Bit 0: Channel 1 lower limit Bit 1: Channel 2 lower limit Bit 2: Channel 3 lower limit Bit 3: Channel 4 lower limit Bit 4: Channel 1 upper limit Bit 5: Channel 2 upper limit Bit 6: Channel 3 upper limit Bit 7: Channel 4 upper limit	00

0203	1	r	Reserved	00
0204	4	r32	Binary data channel 1 (18-bit signed)	00000000
0208	4	r32	Binary data channel 2 (18-bit signed)	00000000
020C	4	r32	Binary data channel 3 (18-bit signed)	00000000
0210	4	r32	Binary data channel 4 (18-bit signed)	00000000
0214	**2**	**w**	**PDO Write**	
0214	1	w	PDO control register Bit 0: Channel 1 enable (1 = channel enabled) Bit 1: Enable channel 2 Bit 2: Enable channel 3 Bit 3: Enable channel 4 Bit 4: Reserved Bit 5: Start synchronous ADC (1 = active) Bit 6-7: Reserved	00
0215	1	w	LED Overwrite Register Bit 0-1: LED channel 1 00 = off (HW status active, no SW overwrite) 01 = Enable SW Overwrite "0" 11 = Enable SW Overwrite "1" 10 = Reserved Bit 2-3: LED channel 2 Bit 4-5: LED channel 3 Bit 6-7: LED channel 4	00
0216	**234**	**r/w**	**SDO**	
0216	2	r w16	Scan rate (µs) The shortest scan rate is defined with 10 µs	000A
0218	1	r/w	Reserved	00
0219	1	r/w	FPGA Oversampling Bit 0-2: Oversampling via FPGA Number of samples = 2^Oversampling Bit 3-7: reserved	00
021A	2	r/w	IIR filter frequency limit channel 1 [Hz] 0 = off, min. 10 Hz	0000
021C	2	r/w	IIR filter frequency limit channel 2 [Hz] 0 = off, min. 10 Hz	0000
021E	2	r/w	IIR filter frequency limit channel 3 [Hz] 0 = off, min. 10 Hz	0000
0220	2	r/w	IIR filter frequency limit channel 4 [Hz] 0 = off, min. 10 Hz	0000

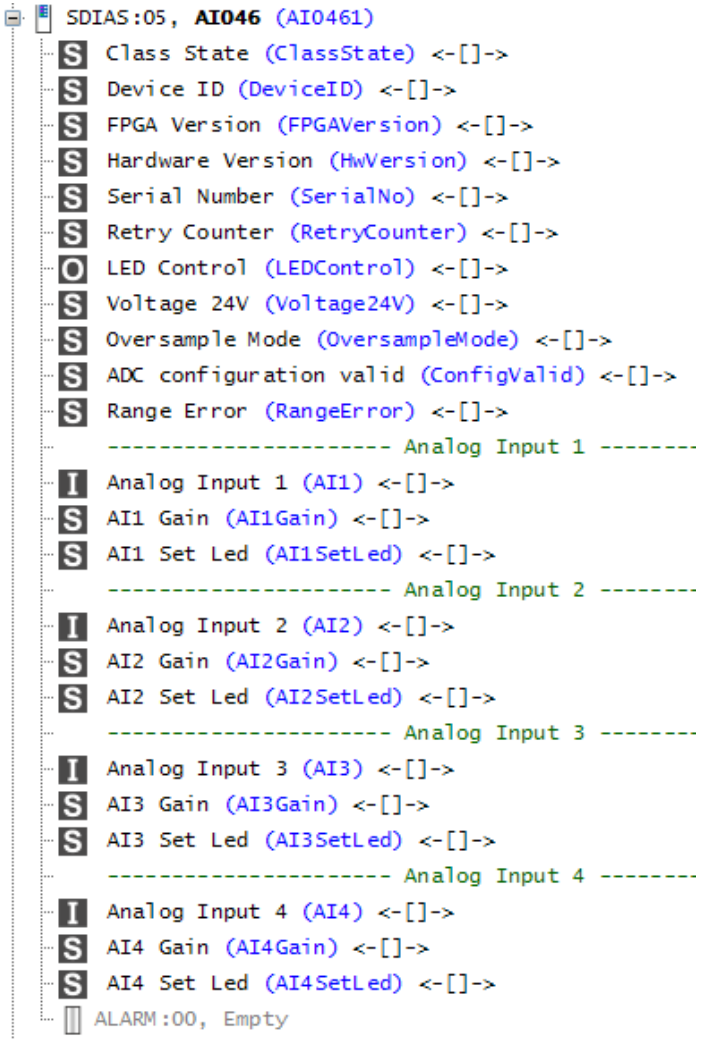
0222	1	r/w	IO Expander Register [1] Bit 2-0: ADC oversampling (value 7 is not supported) Bit 3: ADC reset **For current, 10x amplification is automatically selected and cannot be changed (register value is ignored). For voltage, 1x or 10x can be selected.** Bit 4: Current / voltage amplification channel 1 (0 = 1x, 1 = 10x application) Bit 5: Current / voltage amplification channel 2 Bit 6: Current / voltage amplification channel 3 Bit 7: Current / voltage amplification channel 4	08
0223	1	r/w	Enable lower threshold value of current card (4-20 mA mode) Bit 0: Enable channel (1 = threshold value detection active) Bit 1: Enable channel 2 Bit 2: Enable channel 3 Bit 3: Enable channel 4 Bit 4-7: Reserved	00
0224	4	r/w	Lower threshold value cable break (for current card only) Bit 0-18: Lower threshold value (signed) Bit 10-31: Reserved	00000000
0228	1	r	Error/status register Bit 0: Calibration data could not be read Bit 1: Calibration data (CRC error) Bit 2: IIR filter calculation error (OR gated) Bit 3: Operational (1 = active) Bit 4: Current or voltage measurement (1 = current, 0 = voltage) Detection via Pin wiring / placement variant, filtered Bit 5-7: Reserved	00
0229	1	r/w	SDO control register Bit 0: Value range in data memory 0 = 32-bit access 1 = 18-bit value 1 = 16-bit access 1 = 18-bit value of bits 17...2 Bit 1-5: Reserved Bit 6: Reload configuration (when written as "1") Bit 7: MicroBlaze (µC) Reset (1 = MicroBlaze in Reset)	80
022A	1	r	IIR filter error (latched) Bit 0: Channel 1 overflow Bit 1: Channel 2 overflow Bit 2: Channel 3 overflow Bit 3: Channel 4 overflow Bit 4-7: Reserved	00
022B	213	-	Reserved	-
0300	**48**	**r/w**	**DPRAM (used for buffering calibration data) Amplification 1x**	
0300	4	r/w	Calibration data channel 1 offset	0..0

0304	4	r/w	Calibration data channel 1 multiplier	0..0
0308	4	r/w	Calibration data channel 1 divisor	0..0
030C	4	r/w	Calibration data channel 2 offset	0..0
0310	4	r/w	Calibration data channel 2 multiplier	0..0
0314	4	r/w	Calibration data channel 2 divisor	0..0
0318	4	r/w	Calibration data channel 3 offset	0..0
031C	4	r/w	Calibration data channel 3 multiplier	0..0
0320	4	r/w	Calibration data channel 3 divisor	0..0
0324	4	r/w	Calibration data channel 4 offset	0..0
0328	4	r/w	Calibration data channel 4 multiplier	0..0
032C	4	r/w	Calibration data channel 4 divisor	0..0
0330	**48**	**r/w**	**DPRAM (used for buffering calibration data) Amplification 10x**	
0330	4	r/w	Calibration data channel 1 offset	0..0
0334	4	r/w	Calibration data channel 1 multiplier	0..0
0338	4	r/w	Calibration data channel 1 divisor	0..0
033C	4	r/w	Calibration data channel 2 offset	0..0
0340	4	r/w	Calibration data channel 2 multiplier	0..0
0344	4	r/w	Calibration data channel 2 divisor	0..0
0348	4	r/w	Calibration data channel 3 offset	0..0
034C	4	r/w	Calibration data channel 3 multiplier	0..0
0350	4	r/w	Calibration data channel 3 divisor	0..0
0354	4	r/w	Calibration data channel 4 offset	0..0
0358	4	r/w	Calibration data channel 4 multiplier	0..0
035C	4	r/w	Calibration data channel 4 divisor	0..0

(1) Note: each time the IO Expander Register is written, an access is run and it is updated in the hardware

8 Hardware Class AI046

Hardware class AI046 for the S-DIAS AI 046 analog module



This hardware class is used to control the AI 046 hardware module. The module has four analog inputs with 2048 bytes memory each. The measurement values of each analog input are written into the corresponding memory. More information on the hardware can be found in the module documentation.

8.1 General

ClassState	State	This server shows the actual status of the hardware class.
DeviceID	State	The device ID of the hardware module is shown in this server.
FPGAVersion	State	FPGA version of the module in 16#XY (e.g. 16#10 = version 1.0).
Hardware version	State	Hardware version of the module in format 16#XXYY (e.g. 16#0120 = Version 1.20)
Serial Number	State	The serial number of the hardware module is shown in this server.
Retry counter	State	This server increments when a transfer fails.
LED control	Output	With this server, the application LED of the S-DIAS module can be activated to find the module in the network more quickly. 0 LED off 1 LED on 2 blinks slowly 3 blinks rapidly
Voltage 24 V	State	Shows whether the 24 V supply is OK. 0 not OK 1 OK
Required	Property	This client is active by default, which means that the S-DIAS hardware module at this position is mandatory for the system and can under no circumstances be disconnected or return an error. Otherwise, the entire hardware deactivated. If the hardware module is missing or removed, an S-DIAS error is triggered. If his client is initialized with 0, the hardware module located in this position is not mandatory. This means that it can be inserted or removed at any time. However, which components identified as "not required" should be selected with regard to the safety of the system.

8.2 Analog Inputs [1-4]

Config Valid	State	Shows whether the configuration of analog input 1-4 is valid. 1 configuration is valid 0 configuration is written -1 configuration is not valid
AI[1-4] Analog Input	Input	Analog input. Here, the first value of the according measurement value memory is displayed. The displayed value depends on Gain, MaxValue and MinValue. With open/shorted input the hardware class returns -2147483632 (0x8000 0010).
AI[1-4] Gain	Output	Amplification setting. 0 amplification of 1 1 amplification of 10
AI[1-4] Channel Active	Property	For activating the analog input. 0 analog input is deactivated 1 analog input is activated as initialization value
AI[1-4] Maximum Value	Property	To set the upper scale range. 10 Bit ±110.000 maximum resolution complies with ±11 V 16 Bit ±27.500 maximum resolution complies with ±11 V as initialization value
AI[1-4] Minimum Value	Property	To set the lower scale range. 10 Bit ±110.000 maximum resolution complies with ±11 V 16 Bit ±27.500 maximum resolution complies with ±11 V as initialization value
AI[1-4] IIR Filter Grenzfrequenz	Property	This client sets the filter frequency limit of the software low pass filter. 0 off (default) 1 10 kHz 2 5 kHz 3 1000 Hz (1 kHz) 4 500 Hz 5 100 Hz 6 50 Hz 7 25 Hz 8 10 Hz as initialization value
AI[1-4]LED Overwrite	Output	For activating the status LED. 0 HW status active 1 LED on 2 LED off
Oversample Mode	Output	For setting the oversampling mode. 0 FPGA oversampling 1 ADC oversampling

Samples Per Ms	Property	For setting the samples to be sent per cycle and analog input. The shortest conversion time for the ADC is 10 µs. This results in a maximum of 100 measurement values per millisecond, which can be sent. 0 1 Sample per ms (1 ms conversion time) FPGA OVS … 64 ADC OVS … 64 + FPGA OVS … 2 1 2 Samples per ms (500 µs conversion time) FPGA OVS … 32 ADC OVS … 64 2 4 Samples per ms (250 µs conversion time) FPGA OVS … 16 ADC OVS … 32 3 5 Samples per ms (200 µs conversion time) FPGA OVS … 16 ADC OVS … 32 4 10 Samples per ms (100 µs conversion time) FPGA OVS … 8 ADC OVS … 16 5 20 Samples per ms (50 µs conversion time) FPGA OVS … 4 ADC OVS … 8 6 40 Samples per ms (25 µs conversion time) FPGA OVS …2 ADC OVS …4 7 50 Samples per ms (20 µs conversion time) FPGA OVS …2 ADC OVS … 2 8 100 Samples per ms (10 µs conversion time) FPGA OVS … 1 ADC OVS … 1 as initialization value
Values Size	Property	For setting the size of a measurement value. 0 16 Bit mode (2 byte value) 1 18 Bit mode (4 byte value) (default) as initialization value

8.3 Cable Break Detection

Range Error	State	Shows, whether on the the analog input 1-4 a cable break or over current occurred. An error is also shown by the LED on each single analog input. Detection lower measurement limit (cable break detection): Bit 0 channel 1 lower limit Bit 1 channel 2 lower limit Bit 2 channel 3 lower limit Bit 3 channel 4 lower limit Detection upper measurement limit: Bit 4 channel 1 upper limit Bit 5 channel 2 upper limit Bit 6 channel 3 upper limit Bit 7 channel 4 upper limit

8.4 Communication Interfaces

ALARM	Downlink	With this downlink the corresponding alarm class can be placed via the hardware editor.

8.5 Global Methods

The following method can be called with the server ClassState.

8.5.1 GetData

This function is used to copy data from the measurement value memory.

Transfer parameters	Type	Description
usChannelNr	USINT	Indicates analog input, from which the data should be read.
uiDataLength	UINT	Indicates the required data length in bytes. Per measurement value 2 bytes in the 16-bit mode and 4 bytes in the 18-bit mode are needed.
pBufferData	^void	Pointer to the buffer, where the data of the measurement value memory should be copied to.
pDataCounter	^UDINT	If the pointer is valid and there are no errors in the method, the current data counter is written to its contents to indicate whether there is new data.
Return parameters	**Type**	**Description**
dRetCode	DINT	0 data were copied -1 selected analog input is inactive -2 selected analog input is not available -3 data length is not valid -4 data of the analog input are not valid

8.6 Internal Properties

The shortest conversion time of the ADC is 10 microseconds. In one millisecond, a maximum of 100 values can be thereby converted. If all 4 analog inputs are active, then 400 measurement values per millisecond are processed.

Operation of the module with a bus cycle time below 1 ms is only supported for certain samples per ms:

Bus cycle time samples/ms	50 µs	100 µs	125 µs	200 µ	250 µs	55 µs	≥ 1 ms
1	✓	✓	✓	✓	✓	✓	✓
2	✓	✓	✓	✗	✓	✓	✓
4	✓	✗	✓	✗	✓	✓	✓
5	✓	✓	✗	✓	✗	✗	✓
10	✓	✓	✗	✓	✗	✓	✓
20	✓	✓	✗	✓	✓	✓	✓
40	✓	✓	✓	✓	✓	✓	✓
50	✗	✓	✗	✓	✗	✓	✓
100	✓	✓	✗	✓	✓	✓	✓

✓ supported
✗ not supported

8.6.1 Example: Exceeding the Maximum Memory Size

As the maximum memory size is 2048 bytes, is the 18-bit mode a maximum of 512 measurement values can be recorded.
So with a setting of 100 values per millisecond in the 18-bit mode, the bus cycle time must not be higher than 5 milliseconds. Otherwise the measurement value memory overflows.
With a bus cycle time of 6 milliseconds and activation of only one channel, the following calculation is true:
100 samples * 4 bytes (18-bit) = 400 bytes per channel
400 bytes * 6 milliseconds = 2400 bytes
This configuration is not allowed, as only 2048 bytes read memory are available.

8.6.2 Example: Exceeding the Available Read Memory of the SDIAS Manager

When increasing the bus cycle time also the read memory need increases. A maximum of 6143 bytes read memory can be used,
With a bus cycle time of 4 milliseconds and activation of all 4 channels in the 18-bit mode, the following calculation is true:
100 samples per channel * 4 bytes (18-bit) = 400 bytes per channel
400 bytes per channel * 4 = 1600 bytes with four channels
1600 bytes * 4 milliseconds = 6400 bytes
This configuration is not allowed, as only 6143 bytes read memory are available.

Documentation Changes

Change date	Affected page(s)	Chapter	Note
28.06.2017	5	1.3 Measurement Precision	Info warm up phase deleted Accuracy incl. Calibration error and noise
10.07.2017	4	1.1 Analog Input Specifications	Scan rate, data memory depth per channel, calculation basis, number of values per channel (n) added
	17	6 Configuration	Chapter added
	20	7 Addressing	reworked
14.07.2017	6	1.3 Measurement Precision	Total error added
20.07.2017	3, 4	1.1 Analog Input Specifications	Input filter hardware and footnote 2 changed
	6	1.2 Measuring Modes	Diagram added
10.08.2017			All notes about internal jumper deleted
17.08.2017	9	1.7 Environmental Conditions	Added operating conditions
	13	3.2 Applicable Connectors	Added sleeve length Added info regarding ultrasonically welded strands
11.10.2017	3	1.1 Analog Input Specifications	Common mode range changed to ±6 V
	6	1.3 Measurement Precision	20-40 °C changed to 0,006 %
18.10.2017	15	3.3 Label Field	Added chapter
	19	5 Mounting	Graphic replaced
14.02.2018	1		resolution instead of converter resolution
20.09.2018		3 Connector Layout	Note added
14.11.2019		8 Supported Cycle Times	Chapter added
28.02.2020	26	8 Supported Cycle Times	Text adapted
28.05.2020	26	8 Supported Cycle Times	Chapter removed
08.09.2020		8 Hardware Class AI046	Chapter added
04.11.2020	18	5 Mounting	Expansion functional ground connection