

## C-DIAS Analogue Conversion Module

for eight 0 – 10V DC inputs and  
four  $\pm 10V$  outputs

## CAM 123

This analogue conversion module is a combination of analogue inputs and outputs. There are eight analogue inputs for voltage measurement (0 – 10V / 4 wire) and four analogue outputs for voltage output ( $\pm 10V$ ).

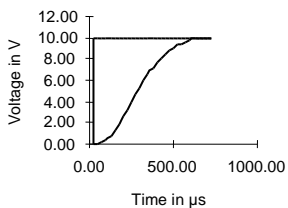


### Technical data

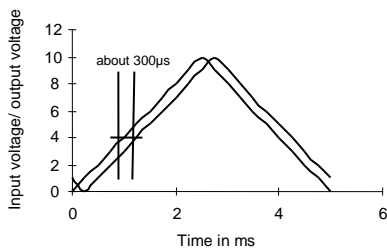
#### Input channel specifications

Number of channels	8 (4 wire connection)	
Measuring range	0 – 10V	
Measured value	0 – 16000	Open input delivers value 16383
Resolution	14 bit	
Transformation time per channel	$\leq 1\text{ms}$	
Input filter	Cut-off frequency 1kHz (1ms)	Low pass class 3
Reference output	$+10V / \pm 1\%$	
Loading capacity of the reference supply voltage per channel	2.5mA	
Precision of the analogue channel	$\pm 0.3\%$ of the maximum measured value	

Response of the input filter CAM 123



Delay of the input signal CAM 123



### Output channel specifications

Number of channels	4
Output voltage	-10 to +10V DC
Output value	-8000 to +8000
Resolution	12 bit (5mV / bit)
Loading capacity of the output voltage	>20K $\Omega$
Protection against short circuiting	Yes
Transient time	<50 $\mu$ s
Refresh time of all channels	<1ms
Precision of the analogue output	$\pm$ 0.4% of the magnitude of the output

**Electrical requirements**

C-DIAS bus supply	+5V / +24V	
Current consumption on the C-DIAS bus (+5V supply)	Typically 30mA	Maximum 50mA
Current consumption on the C-DIAS bus (+24V supply)	Typically 120mA	Typically 150mA

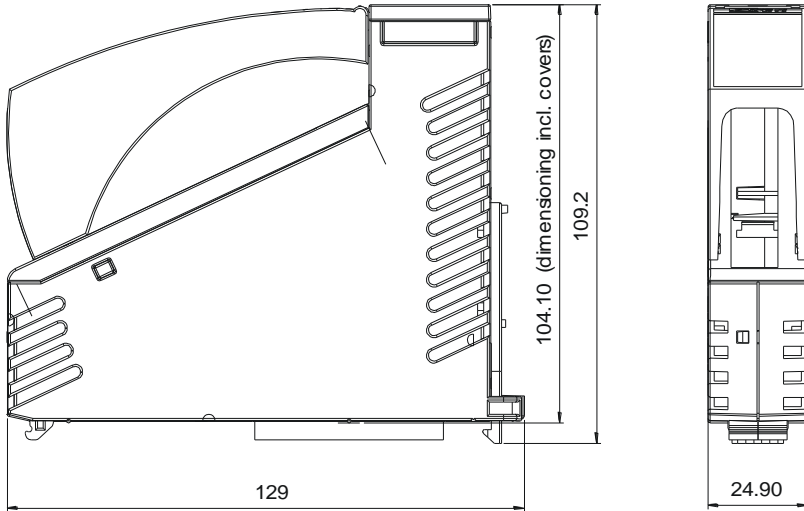
**Miscellaneous**

Article number	12-017-123
Hardware version	3.x
Standardization	UL (E247993)

**Environmental conditions**

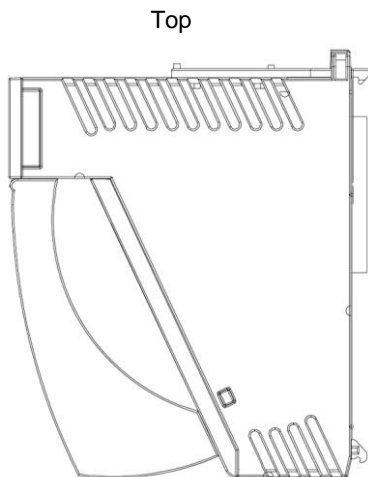
Storage temperature	-20 – +85°C	
Operating temperature	0 – +60°C	
Humidity	0 – 95%, without condensation	
EMV stability	In accordance with EN 61000-6-2 (industrial)	
Resistance to shocks	EN 60068-2-27	150m/s <sup>2</sup>
Protective system	EN 60529	IP 20

## Mechanical dimensions



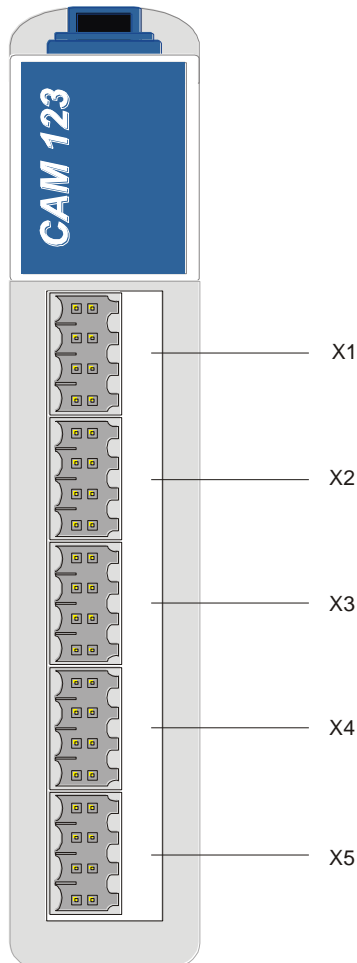
## Mounting position

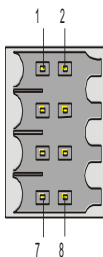
To ensure optimal cooling of the module, the CAM 123 must be mounted as shown (standing). For an angled mounting position, forced convection (cooling fan) must be used.



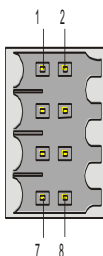
Bottom

## Pin assignment

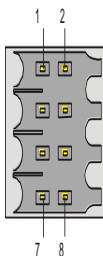


**X1:**


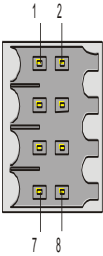
Terminal	Assignment
1	Analogue input 1-
2	Analogue input 1+
3	AGND
4	+10V reference
5	Analogue input 2-
6	Analogue input 2+
7	AGND
8	+10V reference

**X2:**


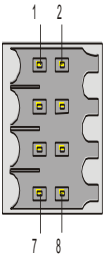
Terminal	Assignment
1	Analogue input 3-
2	Analogue input 3+
3	AGND
4	+10V reference
5	Analogue input 4-
6	Analogue input 4+
7	AGND
8	+10V reference

**X3:**


Terminal	Assignment
1	Analogue input 5-
2	Analogue input 5+
3	AGND
4	+10V reference
5	Analogue input 6-
6	Analogue input 6+
7	AGND
8	+10V reference

**X4:**

Terminal	Assignment
1	Analogue input 7-
2	Analogue input 7+
3	AGND
4	+10V reference
5	Analogue input 8-
6	Analogue input 8+
7	AGND
8	+10V reference

**X5:**

Terminal	Assignment
1	AGND
2	Analogue output 1
3	AGND
4	Analogue output 2
5	AGND
6	Analogue output 3
7	AGND
8	Analogue output 4

**Usable connectors**

**X1-X5:** 8-pole Weidmüller plug B2L3.5/8

The complete C-DIAS plug set CKL 044 with spring clamp is available from Sigmatek with the article number 12-600-044.



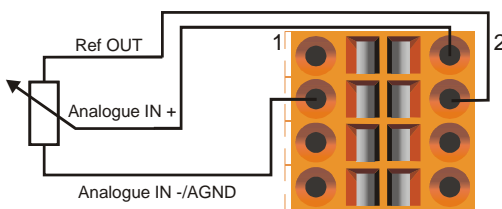
## Wiring instructions

The signals detected from the analogue module are very small in comparison with the digital signals. In order to guarantee trouble free functioning it is essential to stick to a meticulous wiring arrangement:

- The 0V supply voltage connection must follow the shortest path the common 0V terminal.
- The top-hat rail must be properly connected to earth.
- The connecting wires to the sources of the analogue signals must be as short as possible and avoid lying in parallel to wires carrying digital signals.
- The signal carrying wires should be screened.
- The screening must be connected to a common screening rail.

### Voltage measurement with potentiometer (odometry)

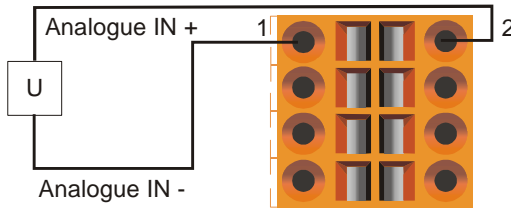
The K- input must be connected to the analogue GND connection.  
(Difference input OFF => K- input is switched to GND per software)



Connection pattern 1

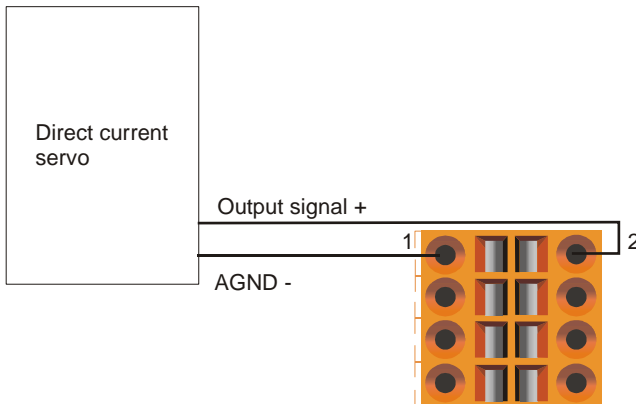
### Active voltage source

With **voltage sources, which are not potential free**, no connection must be made between input and GND or analogue GND.



Connection pattern 2

Example of application: axis control for direct current servos, frequency converter



Connection pattern 3

## Addressing

Address	RD/WR	Function / Bits
\$00	RD16	Analogue measurement value reference voltage 14 bit
\$02	RD16	Analogue measurement value CHANNEL 1, 14 bit, 0 – 10V
\$04	RD16	Analogue measurement value CHANNEL 2, 14 bit, 0 – 10V
\$06	RD16	Analogue measurement value CHANNEL 3, 14 bit, 0 – 10V
\$08	RD16	Analogue measurement value CHANNEL 4, 14 bit, 0 – 10V
\$0A	RD16	Analogue measurement value CHANNEL 5, 14 bit, 0 – 10V
\$0C	RD16	Analogue measurement value CHANNEL 6, 14 bit, 0 – 10V
\$0E	RD16	Analogue measurement value CHANNEL 7, 14 bit, 0 – 10V
\$10	RD16	Analogue measurement value CHANNEL 8, 14 bit, 0 – 10V
\$00	WR16	Analogue output CHANNEL 1, 14 bit, ±10V
\$02	WR16	Analogue output CHANNEL 2, 14 bit, ±10V
\$04	WR16	Analogue output CHANNEL 3, 14 bit, ±10V
\$06	WR16	Analogue output CHANNEL 4, 14 bit, ±10V
\$16	WR8	ADC-DAC configuration: bit 7      10V reference switch on
\$16	RD8	ADC-DAC Status: bit 0              10V reference OK bit 7              10V reference switched on
\$17	RD8/WR8	Difference input ON/OFF Bit 0 = channel 1, bit 1 = channel 2, ..., bit 7 = channel 8 0 = ON, 1 = OFF
\$18	RD8	PLL status register Bit 1 = PLL online Bit 0 = PLL lock (PLL locked)
\$19	RD8/WR8	PLL configuration register Bit 0...3: Period duration of PLL time basis in ms
\$1A	RD8	reserved
\$1B	RD8	Xilinx version

## Matching data (the serial EEPROM is organized byte-wise)

Address	Data	Description
\$00	\$xx	Check sum
\$01	123	Identification
\$02	7	Module group 7=CAM
\$03	2	Module version
\$04	12	Number of channels
\$05	10	Hardware version \$10=HW 1.0
\$06-\$3F	0	FILL
\$10		Serial number
		<b>AI-Matching data 0 – 10V ref way</b>
\$40	\$xxxx	Check sum
\$42	12345	Identification
\$44	28	Length of the following data block in WORD
\$46	8	Number of channels
\$48		A10 Offset = Reference voltage value at the moment of matching
\$4A		A10 Multiplicand not used
\$4C		A10 Divisor not used
\$4E		A11 Offset
\$50		A11 Multiplicand
\$52		A11 Divisor
\$54		A12 Offset
\$56		A12 Multiplicand
\$58		A12 Divisor
\$5A		A13 Offset
\$5C		A13 Multiplicand
\$5E		A13 Divisor
\$60		A14 Offset
\$62		A14 Multiplicand
\$64		A14 Divisor
\$66		A15 Offset
\$68		A15 Multiplicand
\$6A		A15 Divisor
\$6C		A16 Offset
\$6E		A16 Multiplicand
\$70		A16 Divisor
\$72		A17 Offset
\$74		A17 Multiplicand
\$76		A17 Divisor
\$78		A18 Offset
\$7A		A18 Multiplicand
\$7C		A18 Divisor
\$7E-\$7F	0	FILL

<b>AI-Matching data 0 – 10V</b>		
\$80	\$xxxx	Check sum
\$82	12345	Identification
\$84	28	Length of the following data block in WORD
\$86	8	Number of channels
\$88		AI0 Offset = Reference voltage value at the moment of matching
\$8A		AI0 Multiplicand not used
\$8C		AI0 Divisor not used
\$8E		AI1 Offset
\$90		AI1 Multiplicand
\$92		AI1 Divisor
\$94		AI2 Offset
\$96		AI2 Multiplicand
\$98		AI2 Divisor
\$9°		AI3 Offset
\$9C		AI3 Multiplicand
\$9E		AI3 Divisor
\$A0		AI4 Offset
\$A2		AI4 Multiplicand
\$A4		AI4 Divisor
\$A6		AI5 Offset
\$A8		AI5 Multiplicand
\$AA		AI5 Divisor
\$AC		AI6 Offset
\$AE		AI6 Multiplicand
\$B0		AI6 Divisor
\$B2		AI7 Offset
\$B4		AI7 Multiplicand
\$B6		AI7 Divisor
\$B8		AI8 Offset
\$BA		AI8 Multiplicand
\$BC		AI8 Divisor
\$BE-\$BF	0	FILL
<b>AO-Matching data ±10V</b>		
\$C0	\$xxxx	Check sum
\$C2	12345	Identification
\$C4	13	Length of the following data block in WORD
\$C6	4	Number of channels
\$C8		AO1 Offset
\$CA		AO1 Multiplicand
\$CC		AO1 Divisor
\$CE		AO2 Offset
\$D0		AO2 Multiplicand
\$D2		AO2 Divisor

\$D4		AO3 Offset
\$D6		AO3 Multiplicand
\$D8		AO3 Divisor
\$DA		AO4 Offset
\$DC		AO4 Multiplicand
\$DE		AO4 Divisor
\$DF-\$FF	0	FILL