C-DIAS Analog Module CAO 086

For eight ±10 V Outputs

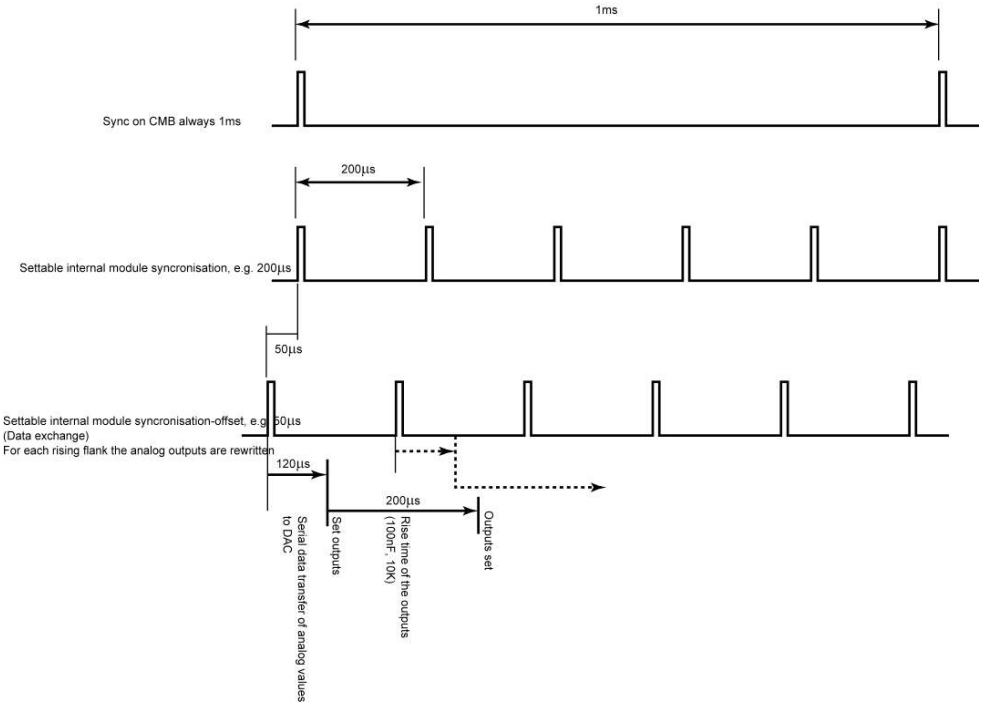
This analog output module can be used to control analog controllable components (i.e.: proportional pressure vent, frequency converter etc.) The analog outputs are galvanically separated from the C-DIAS bus.

Technical Data

Analog channel specification

Number of channels	8	
Output voltage	-10 to +10 V DC	
Output values [Digit]	-30000 to +30000	
Resolution [Bit]	16 Bit	
Resolution [Volt]	333,3 µV / Bit	
Load capacity of output voltage	>10 kΩ (1 mA)	
Capacitive loading of the output voltage	<100 nF	
Short circuit protected	Yes	
Rise time	<200 µs (see rise time sketch)	
Ambient temperature analog channel accuracy (read from the output area)	+20 – +40 °C ±0,025 %	0 – +60 °C ±0,045 %
Status display (up to version 2.0)	Red: PLL is not synchronous, Output defective Yellow: accessing the DAC Green: Galvanically separated supply voltage available.	
Status display (from version 2.0)	Red: Outputs defective Yellow: accessing the DAC Green: Galvanically separated supply voltage available.	

Rise Time



Analog Channel Accuracy

Temperature range field	20 - 40 ℃	0 - 60 ℃
Linearity error	±2 Digit	±2 Digit
Calibration error	±2 Digit	±2 Digit
Temperature influence	±9 Digit	±18 Digit
Deterioration	±2 Digit	±3 Digit
Common error [Digit]	±15 Digit	±25 Digit
Common error [Volt]	±5 mV	±8,4 mV
Common error [%]	±0,025 %	±0,045 %

Electrical Requirements

Supply from C-DIAS-Bus	+5 V and +24 V	
Current consumption of C-DIAS bus (+5 V-supply)	Typically 180 mA	Maximum 200 mA
Current consumption of C-DIAS-Bus (+24 V-supply)	Typically 150 mA	Maximum 200 mA
Galvanic separation (output ←→ C-DIAS-Bus)	500 V (Maximum isolation voltage)	

IMPORTANT:
This module exceeds the standard current consumption for C-DIAS modules!
(+5V: 150mA and +24V: 150mA)

In case this C-DIAS module is mounted on an 8x module carrier (CMB 08x), the total current of the modules used must be determined and tested.
The specification for the current consumption is found in the module specific technical document under “Electrical Requirements”
The total current of the +5V supply cannot exceed 1.2A (150mA/slot).
This also applies to the total current of the +24V supply, which cannot exceed 1.2A (150mA/slot).

IMPORTANT:
La consommation de courant de ce module dépasse les valeurs typiques pour les modules C-DIAS! (+5 V: 150 mA et +24 V: 150mA)

Si ce module C-DIAS est monté sur un fond de panier de taille 8 (CMB 08x), le courant total des modules utilisés doit être déterminé et vérifié.
Les données de la consommation de courant sont mentionnées dans la documentation technique du module respectif dans le paragraphe "Spécifications électriques"
Le courant total de l'alimentation +5 V ne peut pas dépasser 1,2A (150mA/module).
Cela vaut également pour le courant total de l'alimentation +24 V, lequel ne peut également pas dépasser 1,2A (150mA/module).

Miscellaneous

Article number	12-010-086
Hardware version	1.x – 3.x
Standard	UL (E247993)

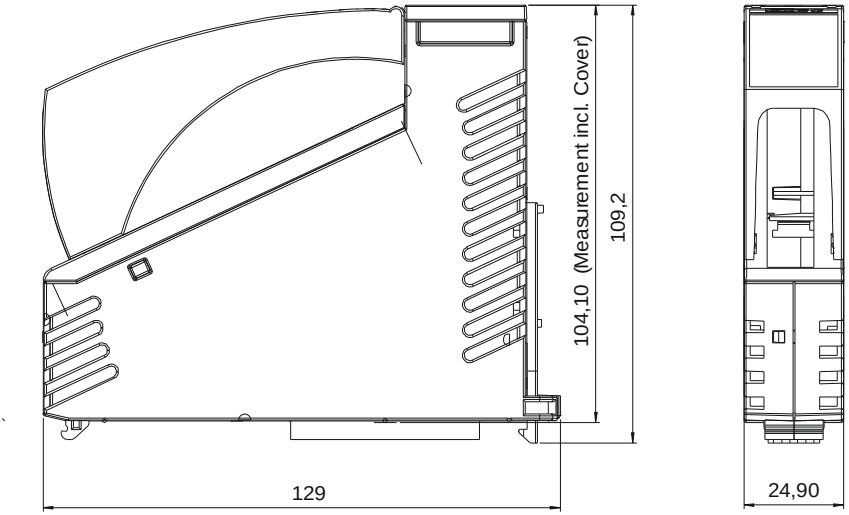
Environmental Conditions

Storage temperature	-30 – +90 ℃	
Operating temperature	20 – +40 ℃ for the above mentioned accuracy	0 – +60 ℃ maximum
Humidity	0 – 95 %, uncondensed	
EMV stability	Per EN 61000-6-2 (Industrial area)	
Shock resistance	EN 60068-2-27	150 m/s²
Protection type	EN 60529	IP 20

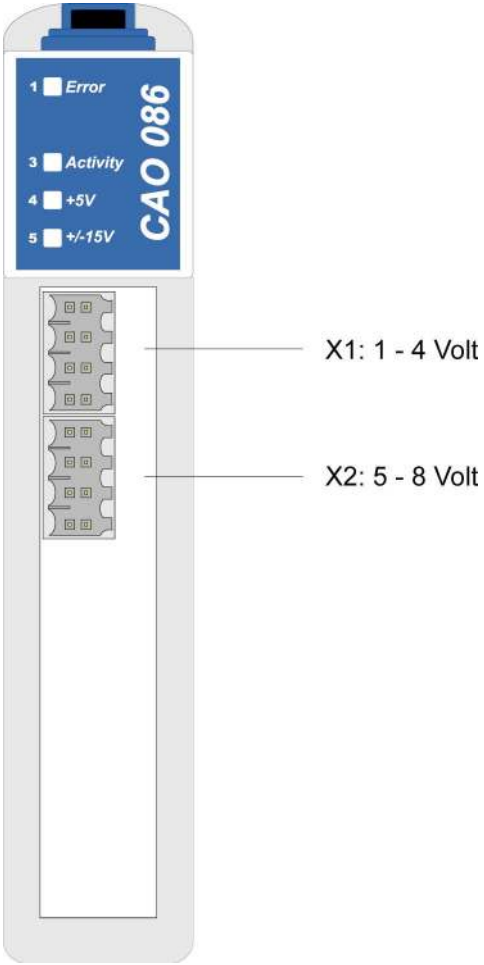
Caution:
Because of the high precision of the analog output module, it must be recalibrated yearly! A minimum of 10 minutes must be allowed for warm up!

Attention:
En raison de la haute précision du module de sortie analogique, il doit être étalonné annuellement! Une période d'échauffement d'au moins 10 minutes est nécessaire!

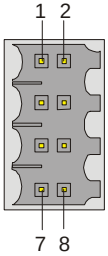
Mechanical Dimensions



Terminal Assignment

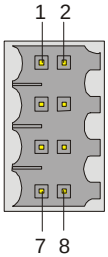


X1: 1 - 4 Volt



Pin	Assignment
1	AGND
2	Analog output 1 (±10 V)
3	AGND
4	Analog output 2 (±10 V)
5	AGND
6	Analog output 3 (±10 V)
7	AGND
8	Analog output 4 (±10 V)

X2: 5 - 8 Volt



Pin	Assignment
1	AGND
2	Analog output 5 (±10 V)
3	AGND
4	Analog output 6 (±10 V)
5	AGND
6	Analog output 7 (±10 V)
7	AGND
8	Analog output 8 (±10 V)

Applicable connector

X1, X2: 8-pol. Weidmüller-plug B2L3,5/8 RM 3,5 gold plated

The complete DIAS connector set CKL 112 with spring terminal is available from Sigmatek under the article 12-600-112.

Status Display

Up to hardware version 2.0

LED No.	LED color	Meaning
1	Red	PLL not synchronous to C-DIAS bus or outputs defective.
3	Yellow	Release of the Analog value
4	Green	+5 V galvanically separated
5	Green	±15 V galvanically separated

From hardware version 2.0

LED No.	LED color	Meaning
1	Red	Outputs defective
3	Yellow	Release of the Analog value
4	Green	+5 V galvanically separated
5	Green	±15 V galvanically separated

Wiring Instructions

To ensure fault free operation, a careful wiring method is recommended:

- The 0 V connection of the voltage supply must be follow the shortest route possible to the 0 V collection point.
- The CMB housing must have a proper earth connection.
- The connection lines to the analog components must be as short as possible and parallel wiring to digital signals must be avoided.
- The signal lines must be shielded.
- The shielding must be connected to a shielding ground bus.

Analog output connection

Example application: Axis control for a DC servo, frequency converter

Addressing

The analog module is not automatically read into the process image.

For the hardware calibration, the calibration data for offset, multiplier and divisor are set at the manufacturer. These values are stored in a serial EEPROM found in the module.

Up to Hardware version 2.0

Address	Access		Function
16#00	WRITE	WORD	Analog value channel 1
16#02	WRITE	WORD	Analog value channel 2
16#04	WRITE	WORD	Analog value channel 3
16#06	WRITE	WORD	Analog value channel 4
16#08	WRITE	WORD	Analog value channel 5
16#0A	WRITE	WORD	Analog value channel 6
16#0C	WRITE	WORD	Analog value channel 7
16#0E	WRITE	WORD	Analog value channel 8
16#10	WRITE	BYTE	Status register Bit 0: 1 = released only when Bit 3 = 1 Bit 1: 1 = released as soon as 16#0F specified Bit 2: 0 Bit 3: 1 = set analog output (see Bit 1)
16#10	READ	BYTE	Bit 0: 1 = released only when Bit 3 = 1 Bit 1: 1 = = released as soon as 16#0F specified Bit 2: 0 Bit 3: 1 = set analog output (see Bit 1) Bit 4: 1 = PLL not synchronous or output defective
16#18	READ	BYTE	PLL Status register Bit 0: 1 = PLL synchronous (to C-DIAS-Sync) Bit 1: 1 = PLL online (C-DIAS-Sync recognized)
16#19	READ WRITE	BYTE	PLL Period (in ms) Default: 1
16#1A	READ WRITE	BYTE	JTAG Master (TDI / TDO, TMS)
16#1B	READ	BYTE	FPGA Version

From hardware version 2.0

Address	Access		Function
16#00	WRITE	WORD	Analog value channel 1
16#02	WRITE	WORD	Analog value channel 2
16#04	WRITE	WORD	Analog value channel 3
16#06	WRITE	WORD	Analog value channel 4
16#08	WRITE	WORD	Analog value channel 5
16#0A	WRITE	WORD	Analog value channel 6
16#0C	WRITE	WORD	Analog value channel 7
16#0E	WRITE	WORD	Analog value channel 8
16#10	WRITE	BYTE	Status register and Start mode Bit 0: 1 = Manual start released only when Bit 3 = 1 Bit 1: 1 = Register Start released as soon as 16#0F specified Bit 2: Cyclic start Output with each cyclic impulse - offset Bit 3: 1 = Set analog outputs (see Bit 1)
16#10	READ	BYTE	Status register and Start mode Bit 0: 1 = Manual start Output only when Bit 3 = 1 Bit 1: 1 = Register Start Output as soon as 16#0F specified Bit 2: Cyclic start Output with each cyclic impulse - offset Bit 4: 1 = PLL not synchronous or outputs defective
16#18	READ	BYTE	PLL Configuration register Bit 0: PLL locked Bit 1: PLL online
16#18	WRITE	BYTE	PLL Configuration register Bit 0 - 7: Register select 0: Offset counter Bit 0 - 7 Register select 1: Offset counter Bit 8 - 9 (Bit 0 - 9 value range: 0 - 950, resolution: 1µs) Register select 2: Period counter Bit 0 - 7 Register select 3: Period counter Bit 8 - 9 (Bit 0 - 9 value range: 0 - 1000, resolution: 1µs)
16#19	READ WRITE	BYTE	PLL Configuration register 1 Bit 0 - 3: PLL period (1 - 15ms) Bit 4 - 6: Register selection for the counter configuration
16#1A	READ WRITE	BYTE	JTAG Master (TDI / TDO, TMS)
16#1B	READ	BYTE	FPGA version

Data in the EEPROM

Module Data (organized by byte)

Address	Data	Description
$00	$xx	Checksum ($00 - $07)
$01	123	Identification
$02	6	Module group 6 = CAO
$03	3	Variant 3 = CAO086
$04	8	Number of channels (8x AO)
$05	$1x	Hardware version $10 = HW-V1.0, $11 = HW-V1.1, …
$06 - $07	0	Free
$08	$xx	Checksum ($08 - $0F)
$09	123	Identification
$10		Serial number
$0A	1	FPGA Family 1 = Xilinx
$0B	1	FPGA Update 1 = Platform flash
$0C	$1A	FPGA Update address LO
$0D	$00	FPGA Update address HI
$0E - $0F	0	Free

AI Calibration Data (organized by Word)

Address	Data	Description
$40	$xxxx	Checksum
$42	12345	Identification
$44	25	Length of the following data blocks in WORD ($44 - $77)
$46	$0008	Number of channels (8x AO)
$48	i.e.: 32776	Offset for 0 V Channel-1
$4A	i.e.: 60000	Gain-Multiplier Channel -1
$4C	i.e.: 65300	Gain-Divisor Channel -1
$4E - $53	-	Calibration value Channel -2
$54 - $59	-	Calibration value Channel -3
$5A - $5F	-	Calibration value Channel -4
$60 - $65	-	Calibration value Channel -5
$66 - $6B	-	Calibration value Channel -6
$6C - $71	-	Calibration value Channel -7
$72 - $77	-	Calibration value Channel -8

Calculation of Analog Values

I.e.:	Offset	32776
	Gain Multiplier	60000
	Gain Divisor	65300

Conversion formula for Analog output

$$DAC\_Value = \frac{Digitalvalue \cdot Gain}{Divisor} + Offset$$

Example:

I.e.: Value for 0 V: $\frac{0 \cdot 60000}{65300} + 32776 = 32776$

Value for -10 V: $\frac{-30000 \cdot 60000}{65300} + 32776 = 5211$

Value for +10 V: $\frac{30000 \cdot 60000}{65300} + 32776 = 60341$