C-DIAS Serial Interface CSI 021

The CSI 021 makes it possible to communicate via 2 independent UART's. 2 x RS232/485/422 outputs are available. These outputs are switchable via software.

Technical data

Performance data

UART controller	16C552
Status display of the Uart	Yes
Transmission rate	50 – 115200 baud
EEProm	Identification on the C-DIAS bus

Electrical requirements

Supply of the C-DIAS bus	+5 V	
Current consumption on the C-DIAS bus (+5 V supply)	Typically 100 mA	Maximum 110 mA

Miscellaneous

Article number	12-012-021
Software Macro	LASAL => Class => CSI021_im PG50 => CSI021.fub
Hardware version	2.x
Standardization	UL (E247993)

Environmental conditions

Storage temperature	-20 – +85 °C	
Operating temperature	0 – +60 °C	
Humidity	0 – 95 %, without condensation	
EMV stability	In accordance with EN 61000-6-2 (industrial)	
Resistance to shocks	EN 60068-2-27	150 m/s²
Protective system	EN 60529	IP 20

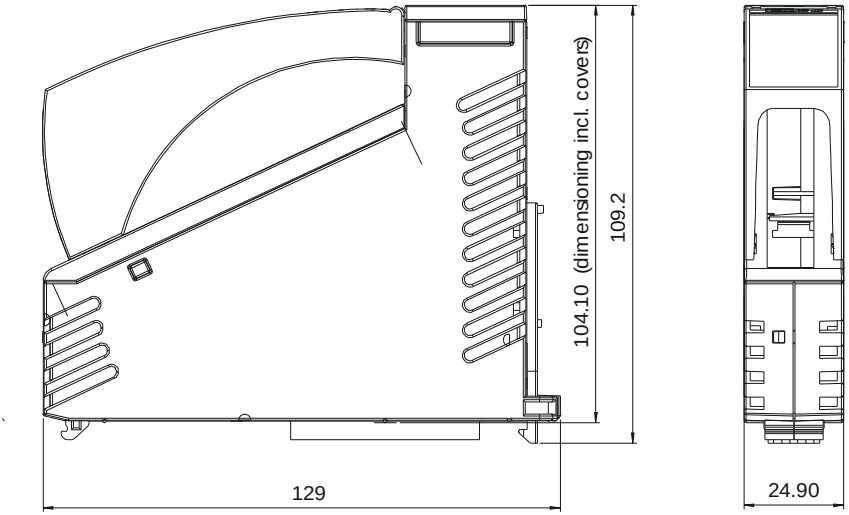
The processor module and the CSI 021 must be placed on the same module carrier!

Le module processeur et le CSI 021 doivent être placés sur le même fond de panier!

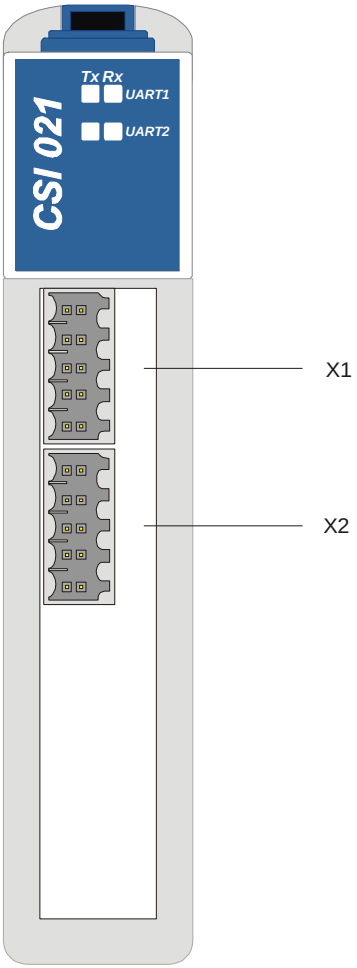
ATTENTION!
At the module carriers CMB 022, CMB 042 and CMB 082 the 32 MHZ clock frequency (CLK) is not provided anymore to the modules. This module requires the clock frequency up to HW version 2.0. A module with a HW version less than 2.0 is only functional with the module carriers CMB 021, CMB 041 and CMB 081!

ATTENTION!
Les fonds de panier CMB 022, 042 et CMB CMB 082 n'offrent pas la fréquence d'horloge de 32 MHz (CLK). Ce module nécessite la fréquence d'horloge de 32 MHz. Il fonctionne donc uniquement avec les fonds de panier CMB 021, 041 et CMB 081!

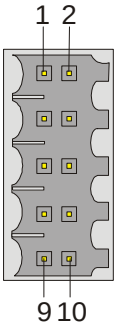
Mechanical dimensions



Connections



X1, X2: RS232/485/422



Pin	RS232	RS485	RS422
1	RxD	RS485 A	TxD +
2	RTS	RS485 B	TxD -
3	TxD	n.c.	RxD +
4	CTS	n.c.	RxD -
5	DTR	n.c.	n.c.
6	GND	GND	GND
7	n.c.	RS485 A	TxD +
8	n.c.	RS485 B	TxD -
9	n.c.	n.c.	RxD +
10	n.c.	n.c.	RxD -

n.c. = do not connect

Useable connectors

X1, X2: 10-pin Weidmüller plug B2L3.5/10

The complete C-DIAS plug set CKL 072 with spring clamp is available from SIGMATEK with the article number 12-600-072.

Wiring Guidelines for RS232

General data / Specifications

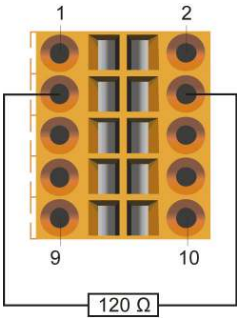
- A data cable with shielding is required!
- Maximum bus stations: 2
- Maximum length: 15 m

Wiring Guidelines for RS422

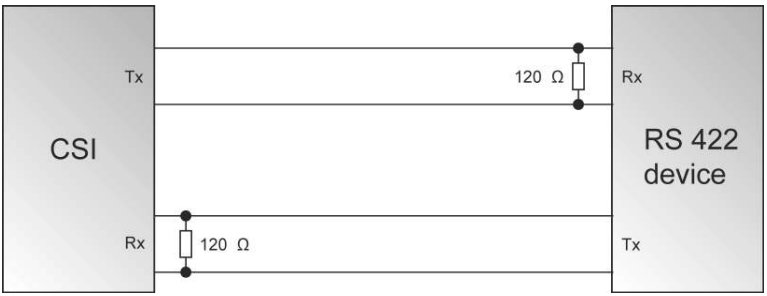
General data/specifications

- A data cable with twisted wires and shielding is required!
- Maximum bus stations: 1 Master, 10 Slaves
- Maximum length: 500 m (ISO Norm 8482)
- Sender / receiver IC: MAX1486

CSI (X1/X2) connection



Wiring

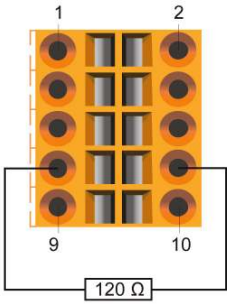


Wiring Guidelines for the RS485

General Data/Specification

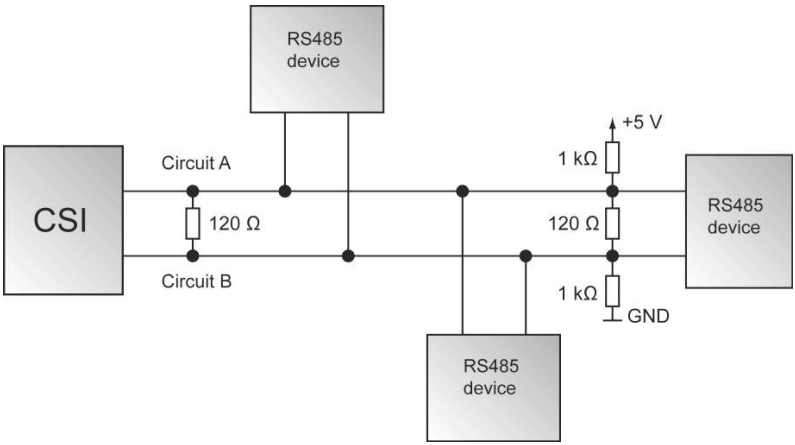
- A data cable with twisted wired and shielding should be used!
- Maximum bus stations: 32
- Maximum length: 500 m (ISO Norm 8482)
- Sender / receiver IC: MAX1486

CSI (X1/X2) connection



Wiring

Since the RS485 requires a Q-level, a pull-up and pull-down termination resistor are needed.



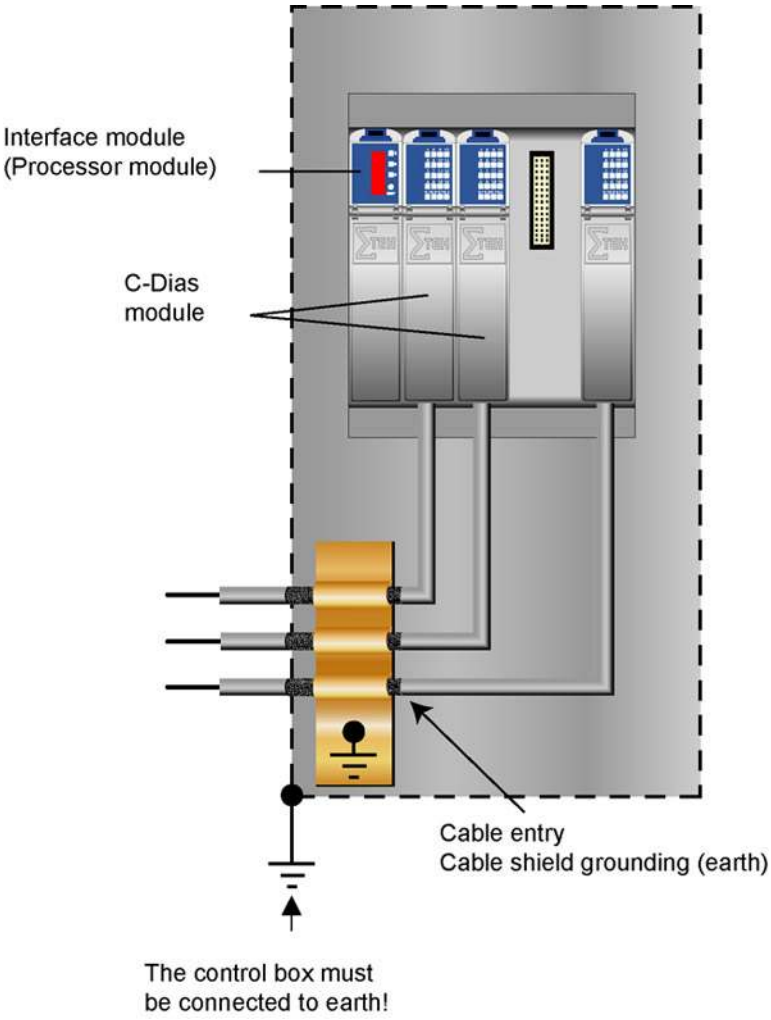
In the graphic above, the 5 V supply is generated externally.

Status display

LED no.	LED color	Meaning
1	Yellow	TX UART 1
2	Yellow	TX UART 2
3	Green	RX UART 1
4	Green	RX UART 2

Wiring Guidelines

To achieve high frequency shielding, both ends of a signal-shielded wire must be connected to earth ground.
For the wiring, caution should be taken to ensure the shield is grounded to earth after the cable entry (at the cable entry would be ideal) so that external disruptions don't reach the module and are redirected over the earth connection.
For this reason the cable insulation is removed and connected to an earth bus. The following graphic illustrates the internal construction of the control box.



Addressing

Address	Access		Function
16#00-07	R/W	Byte	UART 1 PC 16552 see 16552 register table
16#08-0F	R/W	Byte	UART 2 PC 16552 see 16552 register table
16#20	WRITE	Byte	RS 232/422/485 – select register Bit 0: 0 = UART 1 → RS 232 1 = UART 1 → 485/422 Bit 1: 0 = UART 1 → 422 1 = UART 1 → 485 Bit 2: 0 = UART 2 → RS 232 1 = UART 2 → 485/422 Bit 3: 0 = UART 2 → 422 1 = UART 2 → 485 Bit 4-7: reserved
16#F0	WRITE	Byte	IRQ-Enable register: Bit 0: 1 = Enable IO-Interrupt Bit 1: 1 = Enable Com-Interrupt Bit 2: 0 = Interrupt-level 1 = Interrupt-pulse Bit 3-7: reserved
16#F0	READ	Byte	IRQ-acknowledge – Source – Register Bit 0: 1 = IRQ UART 1 Bit 1: 1 = IRQ UART 2

Addressing UART

See data sheet excerpt (PC16552) on the next page!

TABLE II. Register Summary for an Individual Channel

Bit No.	Register Address												
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1	2 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Reg-ister	Divisor Latch (LS)	Divisor Latch (MS)	Alternate Function Register
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM	AFR
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERDAI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8	Concurrent Write
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9	$\overline{\text{BAUDOUT}}$ Select
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1 (Note 3)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10	$\overline{\text{RXRDY}}$ Select
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EMSI)	Interrupt ID Bit (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11	0
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12	0
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13	0
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14	0
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15	0

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the 16450 Mode.

Note 3: This bit no longer has a pin assocated with it.

Data in EEPROM

Module data (organized byte-wise)

Address	Data	Description
$00	$xx	Check sum
$01	123	Identification
$02	20	Module group
$03	1	Version 1
$04	2	Number of channels
$05	$1x	Hardware version $1x = HW-V1.x
$10		Serial number