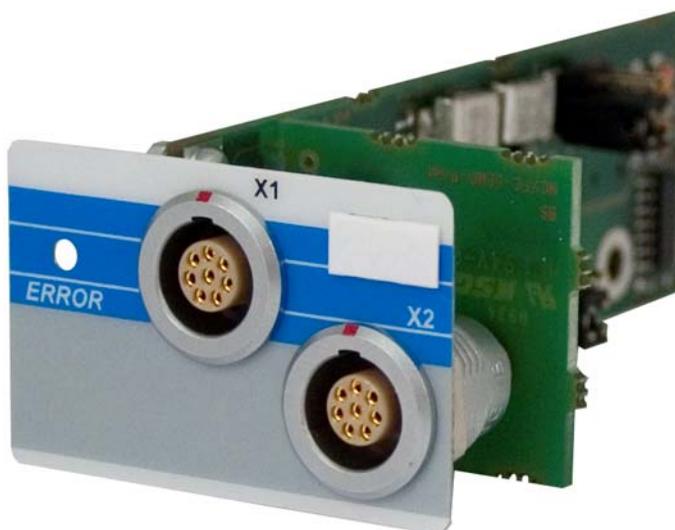# FC Insertable Module   MSR 251

This module has two counter or SSI (Serial Synchronous Interface) inputs. The counters are 32 bits wide and can be used as a counter or frequency meter. The two channels can be configured through the software as counters or an SSI interface. The SSI interface is designed to function as an SSI sensor. Unencoded and Gray encoded sensors are supported.

Technical Data

Counter input

Number of channels	2 counter inputs (or SSI)
Counter width	32 bits
Counter frequency	50 MHz internal 5 MHz external
Time base accuracy	Quartz frequency stability: ±100 ppm, aging: ±5 ppm p.a.

Signal level (Can be selected for each channel using a jumper)	RS422 Inputs: 150 Ohm bus termination, per 1.2 ohm resistor to 5 volts spread and mass	+5 V / 24 V (GND-based) Switching threshold: Typically 2 V Input filter: 50 µs Counter frequency: Max. 10 kHz

Prescaler	16 bits, software configurable	
Pulse suppression	16-bit counter with 1 MHz, software configurable (0 – 65.53 ms in 1 µs steps)	
Configuration	Up/Down	Per software
	Enable	Per software
	Load	Per software
	Flank	Per software
	Counter source	Per software
Inputs	2 inputs, which can be optionally used as counters or SSI data inputs.	
Reference counter	Internal counter with programmable prescaler. If the counter of the respective channel is raised, the reference counter is saved.	

SSI encoder specifications

Number of channels	2 SSI (or 2 counter inputs)
SSI signal level	RS422 Inputs: 150-Ohm bus termination, per 1.2-Ohm spread against 5-volt and mass Outputs: without spread
Shift register frequency	125 kHz – 1 MHz
Shift register length	Maximum 32 bits
Signal evaluation	Gray code or binary

Output voltage

Output voltage	+5 V / Short circuit protected 4.5 V – 5.5 V / 0.1 A 4.0 V – 5.5 V / 0.2 A
Total current 5 V per module	400 mA
Total current 5 V per base	1.6 A
Total current 5 V per system	3 A

CAUTION:
An external supply cannot be connected, rather the modules power supply MUST be used!

The output voltage can be selected for each channel using jumpers (x4).
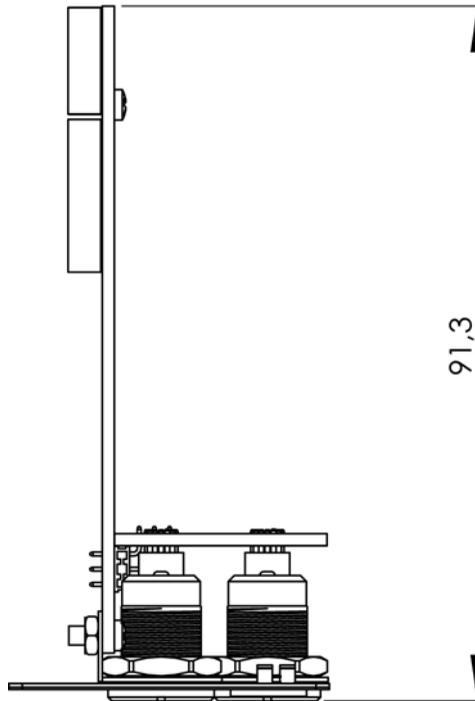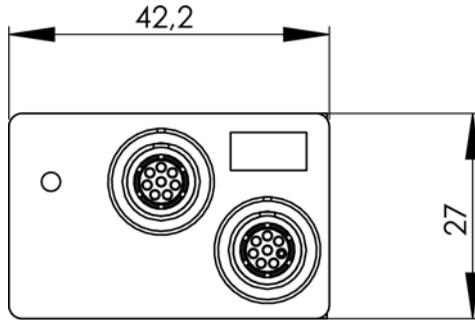**In addition, pads are provided for a 1206 resistor (pull up for an open collector output)**

Miscellaneous

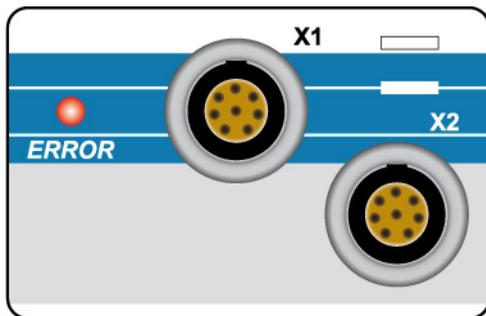| Article number	18-001-251
Hardware version	1.x

Environmental conditions

Storage temperature	-30 – +85 °C	
Operating temperature	0 – +60 °C	
Humidity	0 - 95 %, uncondensed	
EMV stability	According to EN 61000-6-2:2001 (industrial area)	
Shock resistance	EN 60068-2-27	150 m/s²
Protection Type	EN 60529	IP 20

Mechanical Dimensions

Connector Layout

X1: FC 1
Lemo 8-pin (EGG.1B.308.CLN)

Pin	Counter (RS422)	Counter GND (5 V / 24 V)	Counter (SSI)
1	N.c.	N.c.	Serial Clock 1 -
2	N.c.	N.c.	Serial Clock 1 +
3	Counter 1 -	N.c.	Serial Data 1 -
4	Counter 1 +	Counter 1	Serial Data 1 +
5	N.c.	N.c.	N.c.
6	N.c.	N.c.	N.c.
7	GND	GND	GND
8	Output voltage	Output voltage	Output voltage

X2: FC 2
Lemo 8-pin (EGG.1B.308.CLN)

Pin	Counter +/- (RS 422)	Counter GND (5 V / 24 V)	Counter (SSI)
1	N.c.	N.c.	Serial Clock 2 -
2	N.c.	N.c.	Serial Clock 2 +
3	Counter 2 -	N.c.	Serial Data 2 -
4	Counter 2 +	Counter 2	Serial Data 2 +
5	N.c.	N.c.	N.c.
6	N.c.	N.c.	N.c.
7	GND	GND	GND
8	Output voltage	Output voltage	Output voltage

X3: Jumper setting for counters with +/- or GND reference

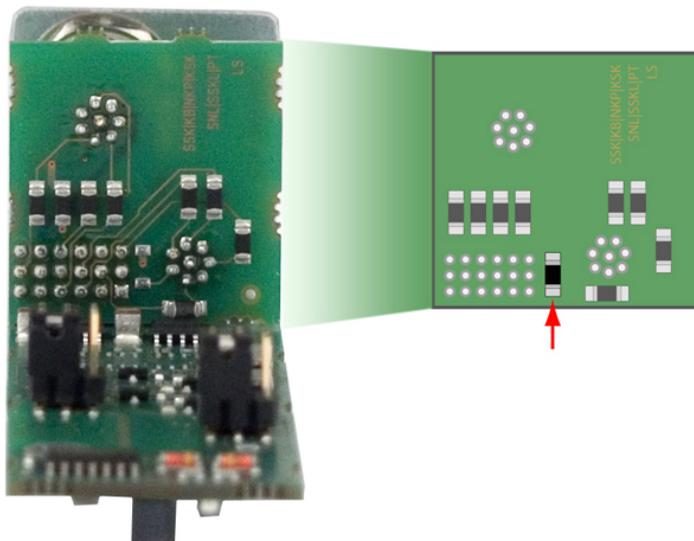Counter +/- (RS422) default setting   Counter GND (5 V / 24 V):

RS 422   5 V / 24 V

Open Collector Output Configuration

MSR 251 Rückansicht Kanal 1
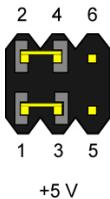

MSR 251 Frontansicht Kanal 2

The resistors are pull-up resistors for the output voltage (5 V or 24 V). If these resistors (type 1206) are placed, a sensor can be connected with an open collector output.

Output voltage +5 V   R ≥ 150 Ω
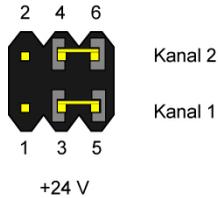Output voltage +24 V   R ≥ 4.7 kΩ

This variant functions with a GND-referenced counter only!

X4: Jumper setting for +5 V or +24 V output voltage

Output voltage +5 V   Output voltage +24 V (default setting)

Kanal 2

Kanal 1

+5 V   +24 V
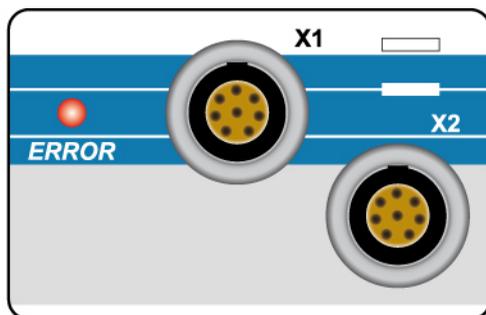

Applicable connectors

X1 - X2:   FGG.1B.308.CLADxx

Applicable connection marker

Weidmüller MultiFit MF 10/5 MC CABUR
Order number: 1854510000

Status display

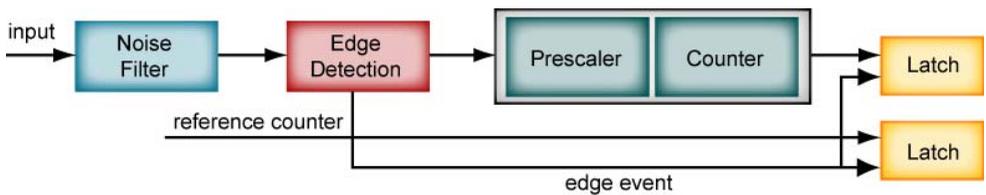| LED number	LED color	Definition
1	RED	Error

Wiring Guidelines

To ensure error-free operation, a careful wiring method must be followed:

* The signal lines must be shielded.

* The shielding must be connected to the connector.

Functions

Block Diagram of a Counter

With the MSR system, 8 counters are available per base module.

Measuring Modes

Both channels are optionally independent of one another and can be used in different measurement modes according to the respective configuration. In the counter mode, the common reference counter for all measuring channels allows temporal relationships between the input signals of several channels to be established.
A configurable digital low-pass filter ("signal suppression" register) can be used to suppress noise signals. The filter is disabled by default (0). With the corresponding configuration, it can be set between 0 and 65,535 ms with a 1 µs resolution through the corresponding configuration.

- Counter mode
    - Period measurement for slow signals
    - Pulse width measurement
    - Period measurement for fast signals
    - Universal counter (pulse counter)

- SSI sensor interface mode
    - Binary mode
    - Gray code decoder mode

Period Measurement for "Slow" Signals

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the count direction UP as well as the internal frequency and flank recognition are selected. The latter allows the period to be measured using a rising or falling flank as a reference point. The difference is in the last detected flank (rising or falling) stored as reference point, which is for example, relevant for measuring the phase comparison between multiple channels. Measuring is started by setting the enable bit in the channel and the reference counter registers.

The measurement results are provided in the counter register of the channel as a 32-bit value with a resolution of 20 ns (time base 50 MHz). If the load value of the counter is set to the (Default) value 0, it must be ensured that the counter value is increased by 1 for calculation of the period and signal frequency in the software! The predefined quartz time base allows, for example, 500 kHz signals to be measured with a resolution of ± 1%.
In addition to the relevance for measuring phase comparisons, the extra counter value reference stored in each channel (also a 32-bit value with a 20 ns resolution (50 MHz time base)) also gives information on the availability of new measurement values.

Pulse Width Measurement

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the count direction UP as well as the internal frequency and flank recognition are selected. The latter allows the time measurement of the high or low section of a square wave signal. The stored reference time, which is relevant for measuring the phase comparison between multiple channels, is the last measured rising flank for the low section or the falling flank for the high section. Measuring is started by setting the enable bit in the channel and reference counter registers.

The measurement results are provided in the counter register of the channel as a 32-bit value with a resolution of 20 ns (time base 50 MHz). If the load value of the counter is set to the (Default) value 0, it must be ensured that the counter value is increased by 1 for calculation of the high and low periods in the software! In addition to the relevance for measuring phase comparisons, the extra counter value reference stored in each channel (also a 32-bit value with a 20 ns resolution (50 MHz time base)) also gives information on the availability of new measurement values.

Period Measurement for "Fast" Signals

The period and frequency measurements for fast signals are based on a gate time measurement (average of the counted signal pulses divided by the measurement time).
In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the count direction UP as well as the internal frequency and flank recognition are selected. The 2-flank evaluation setting doubles the measurement resolution.
The stored reference point, which is for example, relevant for measuring the phase comparison between multiple channels, is the last measured rising or falling flank (depending on how the flank evaluation is configured). Measuring is started by setting the enable bit in the channel and reference counter registers.

The measurement result, the number of measured pulses, is provided in the count value register of the channel as a 32-bit value and the corresponding reference counter value is provided in the reference counter register. The result of the period or frequency measurement can be calculated from the difference between the actual and last counter values as well as the difference between the actual and last reference counter values. The gate time is generated from the time between the readings of two measurement values. The measurement channel for the stored reference counter value is latched while reading so that data consistency is ensured. The read-time jitter therefore does not affect the measurement.

Universal Counter (pulse counter)

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the external frequency is selected. Depending on the application, the counter can be configured as an incremental or decremental counter. It can be set to a predefined load value – from which the activated counter immediately continues to count up or down. With enable, starting or stopping is possible at anytime.

The configurable prescaler allows the counter to increment or decrement with every n^{th} pulse (n = 1 to 65535; 0 is 65536). The reference counter is equipped with a configurable prescaler. It should be taken into account that the setting for the prescaler factor affects the reference counter register of all channels.

For exact synchronization of the counter values read from several channels, the latches for the counters and reference counters of all channels can be switched to Hold (see register 16#F7). This keeps the counter status of the various channels from changing while reading. After the required data has been read, the latches re-enabled.

SSI Sensor Interface

In the channel configuration register, the SSI mode is selected and in "SSI shift register length", the total bit stream length specified by the SSI sensor (SSI data, including additional bits such as overflow, power failure…) is selected. In the "SSI shift register frequency and Gray code decoding" register, the desired clock rate (to select the clock rate, see the SSI sensor data sheet) is defined. The cyclic reading of the SSI sensor is activated by the SSI-Start bit in the "configuration and SSI status" register. It should be taken into consideration that the clock rate multiplied by the shift register length and added to the sensor time t_m results in the minimum read time. The interface logic stops a new SSI cycle from being started before the last cycle has been completed (the SSI status bit indicates whether cycle is currently active). Additionally, the maximum measurement rate of sensor must be considered and depending on the effect (incorrect or old values are read, the sensors are synchronized…), the measurement values can't or should not be exceeded. To start a new SSI frame, SSI-Start must be set to 1. The SSI frame is then started with the next cycle (cycle time is determined by the Sub Millisec counter) – as long as the last frame as been completed. SSI-Start is reset automatically; this means that the frame must be started explicitly before each desired cycle.

For flexible adjustment to the sensor element, the SSI read cycles can be individually started by configuring "PLL configuration register" and "PLL counter configuration register".

Binary mode

For the binary mode, the Gray code decoding (default: on) must be enabled. This mode is also recommended if the sensor provides data but contains additional unencoded bits, which would lead to falsified data during automatic decoding. Decoding must be performed in the software. The deserialized data stream is provided as a 32-bit value in the "SSI data " register.

Gray code decoder mode

For sensors that provide Gray encoded data. The result is decoded automatically (Gray code decoding on) and provided as a 32-bit value in the "SSI data" register. In this mode, the additional bits in the sensor-data stream must be taken into consideration. With additional bits that are not encoded and transmitted in the serial data stream before the coded measurement data, the decoding leads to corruption of all data. With additional bits that are not encoded and transmitted in the serial data stream after the coded measurement data, the decoding leads to corruption of the additional bits.