

## VARAN Client Board

## VEB 011-SPI

Versatile Automation Random Access Network

This client board is used to easily equip any periphery device with the VARAN bus. Data can be exchanged over an alternating buffer and DPRAM.



# 1 Technical Data

## 1.1 Performance Data

Internal memory	4-Mbit serial Flash
Interfaces	1 x VARAN (Client) 1 x Periphery interface
Connection to periphery device	Over 50-pin board-to-board connector, 0.8 mm spacing (Type ERNI Microstac, order Nr. 114713)

## 1.2 Electrical Requirements

Internal power supply (VDD)	Typically +3.3 V DC ( $\pm 4\%$ ) (Provided from the periphery module over a 50-pin connector)
Current consumption of voltage supply	Minimum 250 mA (Depending on the external circuit)

## 1.3 Miscellaneous

Article number	16-081-011-SPI
Hardware version	1.x

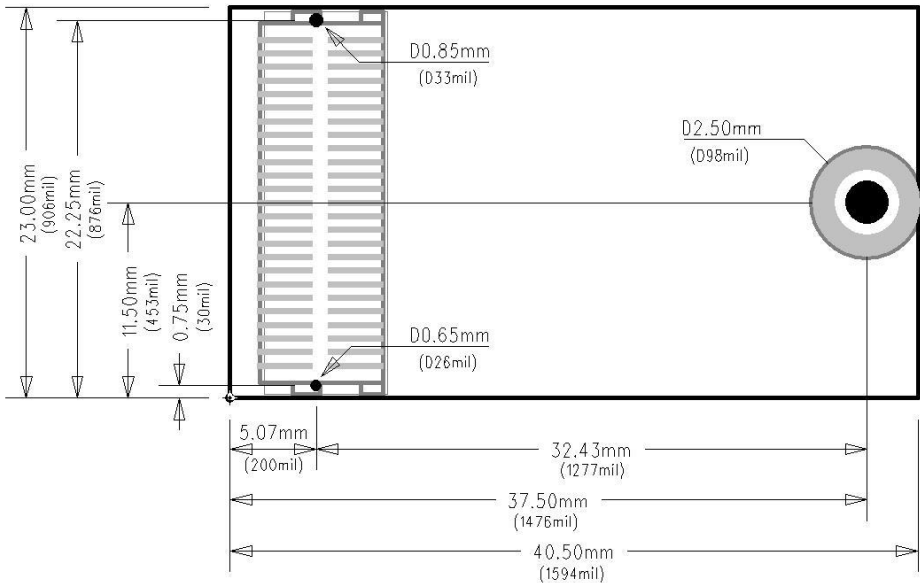
## 1.4 Environmental Conditions

Storage temperature	-20 – +85 °C
Operating temperature <sup>(1)</sup>	0 – 70 °C
Humidity	0 - 95 %, non-condensing
EMC stability	<sup>(2)</sup>
Shock resistance	150 m/s <sup>2</sup>

<sup>(1)</sup> According to component specifications. The operating temperature for the entire unit must be specifically defined for each application, as the operating conditions (mounting position, housing, heat sources in the vicinity of the VEB) are unknown.

<sup>(2)</sup> For each application, the EMC resistance must be tested separately in the entire system.

## 2 Mechanical Dimensions



The dimensioning of the center holes in the 50-pin ERNI board-to-board connector plug align with connector on the base card (does not show the position of the connector on the VEB)

The VEB in the above drawing is visible from the rear of the connector.

The component height on the base card under the VEB cannot exceed 3 mm.

### 3 Basics

The present document is intended for the programmer. It should contain all required information to create a program or client.

### 3.5 Connectors

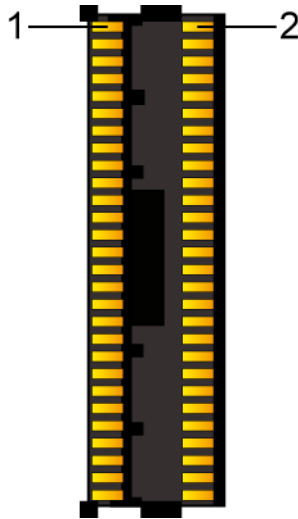


Image 1: Connectors

## 4 Programming

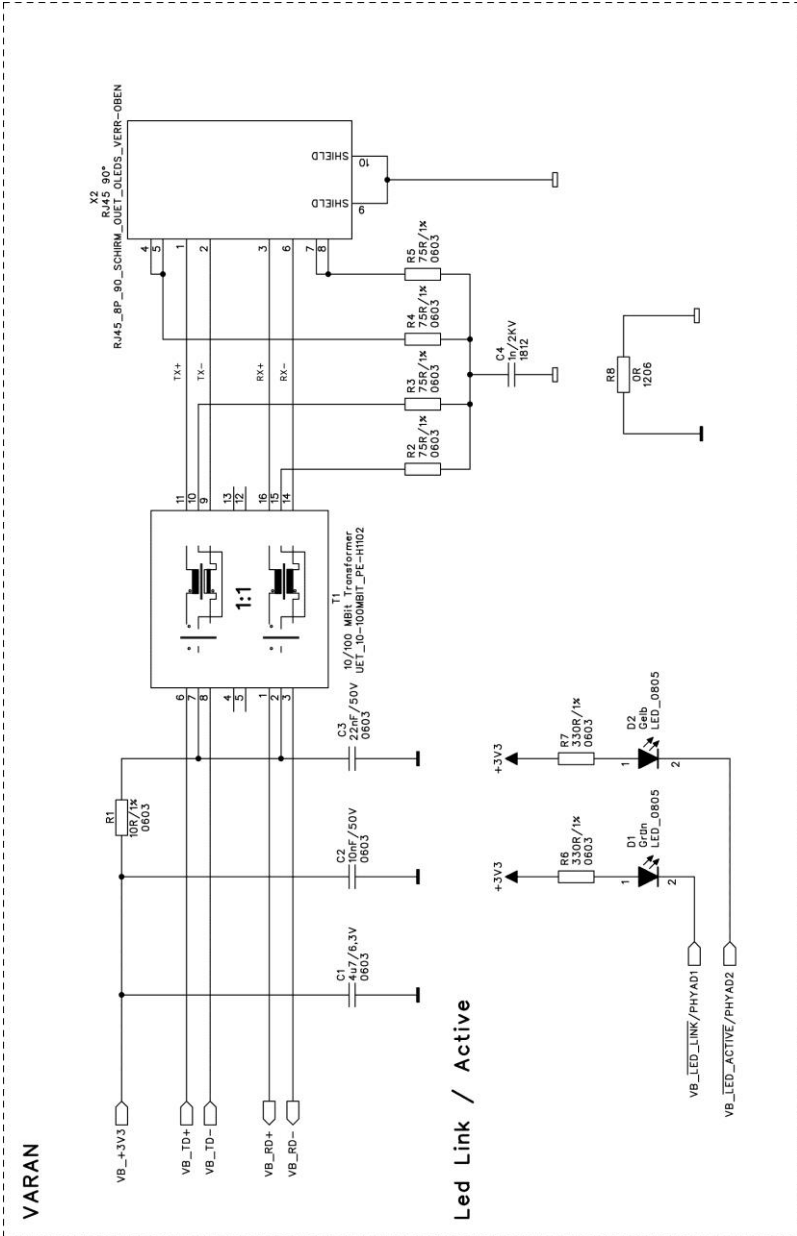
### 4.1 VEB 011-SPI Pin Layout

PIN	Identifier	Function	
1	GND	Ground	-
2	GND	Ground	-
3	mosi	SPI Data In	In
4	miso	SPI Data Out	Out
5	sck	SPI Clock	In
6	-	-	-
7	$\overline{\text{ssel}}$	SPI Chip Select	In
8	-	-	-
9	-	-	-
10	-	-	-
11	-	-	-
12	veb_irq	IRQ	Out
13	-	-	-
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	VDD	+3V3 supply	In
20	VDD	+3V3 supply	In
21	GND	Ground	
22	-	-	-
23	VB_RD+	RX+ transmitter	-
24	veb_sync	Sync	Out
25	VB_RD-	RX- transmitter	-
26	dig_in(0)	Digital Input	In1
27	VB_TD+	TX+ transmitter	-
28	dig_in(1)	Digital Input	In2
29	VB_TX-	TX- transmitter	-

30	dig_in(2)	Digital Input	In3
31	-	VB +3V3	Out
32	dig_in(3)	Digital Input	In4
33	clk_25mhz_out	CLK 25 MHz	Out
34	dig_in(4)	Digital Input	In5
35	periphery_reset	Periphery Reset	Out
36	dig_in(5)	Digital Input	In6
37	-	-	-
38	dig_in(6)	Digital Input	In7
39	dig_out(7)	Digital Output	Out8
40	dig_in(7)	Digital Input	In8
41	dig_out(5)	Digital Output	Out6
42	dig_out(6)	Digital Output	Out7
43	-	LED	Out
44	dig_out(4)	Digital Output	Out5
45	-	LED	Out
46	dig_out(3)	Digital Output	Out4
47	dig_out(1)	Digital Output	Out2
48	dig_out(2)	Digital Output	Out3
49	GND	Ground	
50	dig_out(0)	Digital Output	Out1

**Table 1: Pin layout**

## 4.2 Electrical bonding





## 4.3 Layout Guidelines

- Place blocking capacitors with 100 nF to the supply pins (+3V3) of the Board-to-Board connectors.
- The distance between the transformer (Pulse H1102NLT) and the RJ45 plug connector has to be kept to a minimum (<25 mm)
- The distance between the transformer and the 50-pole VEB plug should not exceed 50mm, if possible.
- The VARAN differential lines TD+/TD- and RD+/RD- are
  - as short as possible
  - parallel
  - of same length
  - ... to route
- Furthermore differential lines should have the following properties:
  - Distance between two differential line pairs >0,38 mm
  - Distance of the differential lines to the circuit board angles >25 mm
  - Distance of the differential lines to other signals >0,76 mm
  - Continuous GND area under the differential lines
  - Do not cross differential lines with other signals
  - Do not route differential lines under components

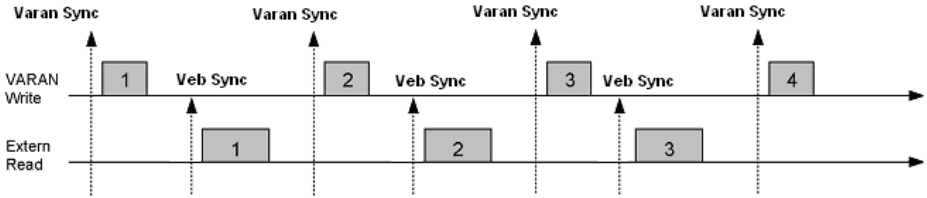
If the VEB 011-SPI is operated on a VEB 021 board, the following signals can be accessed through the multi-pin connector of the VEB 021 board:

VEB 021		VEB 011	
Pin	Label	Pin	Function
1	V1	4	MISO
2	V2	3	MOSI
3	V3	6	-
4	V4	5	SCK
5	V5	8	-
6	V6	7	SSEL
7	V7	10	-
8	GND	1, 2, 21, 49	GND
9	V8	9	-
10	V9	12	IRQ
11	V10	11	-
12	V11	14	-
13	V12	13	-
14	V13	16	-
15	GND	1, 2, 21, 49	GND
16	V14	15	-
17	V15	18	-
18	V16	17	-
19	V17	22	-
20	V18	24	Sync
21	V19	26	In1
22	GND	1, 2, 21, 49	GND
23	V20	28	In2
24	V21	30	In3
25	V22	32	In4
26	V23	34	In5
27	V24	33	CLK 25 MHz
28	V25	36	In6

29	GND	1, 2, 21, 49	GND
30	V26	35	Periphery RESET
31	V27	38	In7
32	V28	37	-
33	V29	40	In8
34	V30	39	Out8
35	V31	42	Out7
36	GND	1, 2, 21, 49	GND
37	V32	41	Out6
38	V33	44	Out5
39	V34	46	Out4
40	V35	48	Out3
41	V36	47	Out2
42	V37	50	Out1
43	GND	1, 2, 21, 49	GND
44	GND	1, 2, 21, 49	GND
45	+3V3	19, 20	+3V3
46	+3V3	19, 20	+3V3

**Tabelle 2: Pinbelegung VEB 021\_011**

### 4.3.1 Timing the Synchronous Manager to the Client (Alternating Buffer)



**Image 2: Client reads data from the Manager, synchronous operation**

The  $\mu\text{C}$  (SPI Master) must be synchronous to the VARAN system.

## 4.4 Address Mapping

### 4.4.1 VARAN Side

Address (hex)	Size (bytes)	Access Type	Description	Reset value
Memory				
0000	2048	w	Alternating Buffer(Write Space) Default = switch by sync, switch mode can be changed in the register	00
0800	2048	r	Alternating Buffer (Read Space) Default = switch by sync, switch mode can be changed in the register	00
1000	512	r/w	reserved	00
1200	1	r	VEB Sync Mode Register Bit 0: 1 = Enable Sync Quitting Mode 0 = Enable Pulse width Register Bit 1: 1 = Sync / veb_irq output is active low, 0 = active high Bit 2: 1 = Enable tristate buffer for sync / veb_irq output Bit 3: Sync Output Register (read) Bit 7..4 : Reserved	00
1201	3	r/w	Reserved	00
1204	4	r/w	VARAN Bus Cycle Time [10 ns]	00000000
1800	2048	r/w	DPRAM	

**Table 3: Address Mapping Varan Manager**

#### 4.4.2 $\mu$ C Side

Address (hex)	Size (bytes)	Access Type	Description	Reset value
0000	2048	r	Alternating Buffer (Read Space) Default = switch by sync, switch mode can be changed in the register	00
0800	2048	w	Alternating Buffer (Write Space) Default = switch by sync, switch mode can be changed in the register	00
1000	256	r/w	Transmit/Receive Buffer	-
1100	2	r/w	Page Address Two higher bytes of SPI address (A23... A8)	0000
1102	1	r/w	Predefined Command Register 16#01: Page Read 16#02: Page program 16#03: Sector Erase 16#F0: Reboot FPGA	00
1103	1	r/w	Single Command Register	00
1104	1	r	Status Register Bit 0: 1=Ready, 0=Busy	01
1105	1	w	Request Register Bit 0..3: Software Request (highest priority) Bit 4..7: Hardware Requests (Bit 7 lowest priority)	-
1106	1	r	Grant Register Bit 0..3: Software Grant Bit 4..7: Hardware Grants	00
1107	1	w	Clear Request Register Bit 0..3: Software Request Bit 4..7: Hardware Requests	-
1108	248	r/w	reserved	
1200	1	r/w	VEB Sync Mode Register Bit 0: 1 = Enable Sync Quitting Mode 0 = Enable Pulse width Register Bit 1: 1 = Sync / veb_irq output is active low, 0 = active high Bit 2: 1 = Enable tristate buffer for sync / veb_irq output  Bit 3: Sync Output Register (read) Bit 6..4: Reserved Bit 7: 1 = Enable Sync clear 1 clock cycle (write) 0 = Disable Sync clear (write)	00
1201	1	r	PLL Frame Counter	00

1202	2	r/w16	Sync Pulse width Register Bit 15..0: Value in steps of 20 ns (e.g. 5 = 100ns and 0 = disabled)	0000
1204	4	r	VARAN Bus Cycle Time [10 ns]	00000000
1208	8	r/w	Reserved	00
1210	1	r/w	Digital In/Output Register	00
1211	239	-	Reserved	-
1300	4	w32	Transmit FIFO Data Input	-
1304	4	w32	Transmit FIFO Frame Length Write frame length before filling the FIFO Bit 10..0: Frame Length (in Bytes max. 1518)	-
1308	4	r32	Receive FIFO Data Output	-
130C	4	r32	Receive FIFO Frame Length (in Bytes) 0 = no valid frame in FIFO	00000000
1310	4	r	Available Registers in Transmit FIFO (in Bytes)	00000000
1314	4	w	FIFO Control register Bit 0: 1 = Reset Transmit FIFO Bit 1: 1 = Reset Receive FIFO	-
1314	4	r	FIFO Status register (IRQ Quit register) Bit 0: 1 = frame transmitted Bit 1: 1 = frame received (valid frame is in FIFO) Bit 2: 1 = transmit FIFO error (Transmit FIFO Frame Length > 1518, or writing false values of bytes in FIFO) Bit 3: 1 = receive FIFO error (Read Receive FIFO when no valid frame)	00000000
1318	4	r/w	Interrupt enable register Bit 0: 1 = frame transmitted Bit 1: 1 = frame received Bit 2: 1 = transmit FIFO error Bit 3: 1 = receive FIFO error	00000000
131C	4	r/w	Receive MAC Filter register Bit 0: 1 = Unicast enable (Destination address = MAC address) Bit 1: 1 = Broadcast enable (Destination address = 16#FFFFFFFFFFFF) Bit 2: 1 = Promiscuous enable (all destination address are received)	00000000
1320	6	r/w	MAC Address	00000000 0000

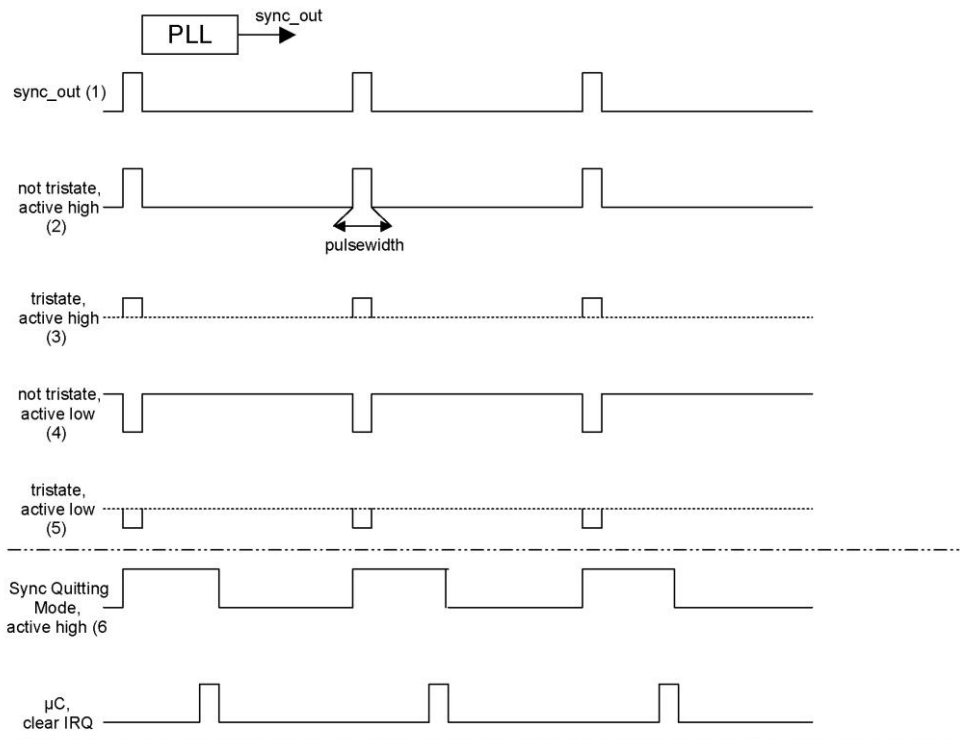
1326	1	r/w	Port Control / Link Status register Bit 0: 1 = Link established (read only) Transmitting is only allowed, when Link is established Bit 1: 1 = Port enable (Port must be enabled before transmitting)	00
1327	1241	r/w	reserved	
1800	2048	r/w	DPRAM	00

**Table 4: Address Mapping  $\mu$ C Client**



## 4.5 Sync Modes

The Sync Mode register allows the synchronization response to be modified.



As can be seen in line 2 and 4, a distinction is made between active high and active low (bit 1). The Sync Quitting Mode can be activated (bit 0). In this case, the µC sends a response as defined in 6.

To avoid damage to the output driver, the tristate buffer option (bit 2) can be activated (3 and 5).

Bit 0 of the Sync Mode register can also activate the pulse width register. Values can be set in 20 ns increments.

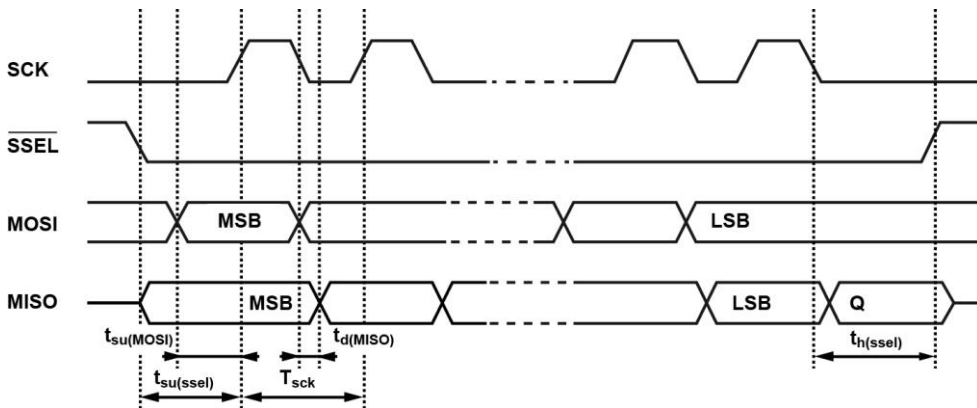
To use the sync interrupt and alternating buffer, the internal PLL must first be activated. This is located in the control area at address 0x0140. 0x01 must be written to address 0x17 of the PLL in order to activate it.

## 4.6 Interrupt Output

The VEB 011-SPI interrupt output can be configured over the same register as the Sync for low-active, high-active and/or tristate. If an interrupt is triggered, the output is then active. The VEB IRQ is controlled through the EMAC. The interrupt must be acknowledged in the respective register to deactivate the interrupt output (e.g. EMAC FIFO Status register - IRQ Quit register)

## 5 External Timing

### 5.1 SPI Access



MSB ... Most significant Bit

LSB ... Least significant Bit

Q ... Undefined

Time setting	Time (ns)		Description
	Min.	Max.	
$t_{su}(sSEL)$	20	-	SSEL low to SCK high
$t_{su}(MOSI)$	0	-	SCK high to read
$t_d(MISO)$	-	80	SCK low to write
$T_{sck}$	200	-	SPI clock period
$T_{h}(sSEL)$	20	-	SSEL Hold time to SCK low

**Table 5: Time characteristics**

The data are recorded with the first rising SCK flank and sent with the falling SCK flank.

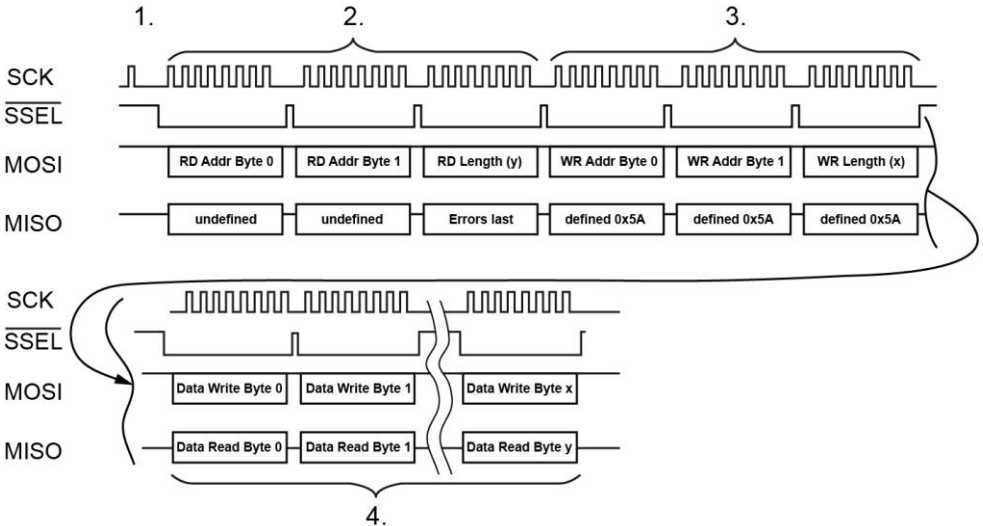
In IDLE status, the SSEL is set to HIGH.

SPI frames always have 8 bits. The maximum SPI pulse frequency is 5 MHz.

## 5.2 SPI Protocol

The SPI protocol consists of 4 parts:

1. Synchronization (optional)
2. Header: Definition of the data that is read from the FPGA
3. Header: Definition of the data that is written to the FPGA
4. Data transfer



### 5.2.1 General description of VEB011-SPI interface

MOSI (VEB011-SPI Input): SPI data input signal

MISO (VEB011-SPI Output): SPI data output signal

SCK (VEB011-SPI Input): SPI clock input signal

/SSEL(VEB011-SPI Input): SPI chip select (active low signal)

=> Data communication between the HOST and the VEB011-SPI uses byte quantities, that is 8 bits.

=> Bit synchronization is done using /SSEL.

=> The most significant bit (MSB) is transferred first.

=> MOSI (VEB011-SPI Input) is sampled at the rising edge of the SCK signal.

=> MISO (VEB011-SPI Output) is changed at the falling edge of the SCK signal.

=> SCK (VEB011-SPI Input) has active high level.

The protocol used in communication between the HOST and the VEB011-SPI consists of a 6 byte header followed by the amount of data specified in the header.

**Master Out Slave In signal (MOSI)**

HDR byte 1: RD addr byte 0 (LSB)  
 HDR byte 2: RD addr byte 1 (MSB)  
 HDR byte 3: RD length byte (0-255)  
 HDR byte 4: WR addr byte 0 (LSB)  
 HDR byte 5: WR addr byte 1 (MSB)  
 HDR byte 6: WR length byte (0-255)  
     WR data byte 0  
     WR data byte 1  
     WR data byte 2  
     WR data byte 3  
     WR data byte 4  
     WR data byte 5  
     WR data byte 6  
     ...

**Master In Slave Out signal (MISO)**

HDR byte 1: undefined value  
 HDR byte 2: undefined value  
 HDR byte 3: errors (in previous data transfer)  
 HDR byte 4: defined 0x5A  
 HDR byte 5: defined 0x5A  
 HDR byte 6: defined 0x5A  
     RD data byte 0  
     RD data byte 1  
     RD data byte 2  
     RD data byte 3  
     RD data byte 4  
     RD data byte 5  
     RD data byte 6  
     ...

The header bytes must be followed by the correct amount of data bytes as specified in HDR byte 3 and HDR byte 6. The correct amount of data bytes can be calculated as the maximum of 'RD length byte' and 'WR length byte'.

Note: If 'RD length byte' is smaller than 'WR length byte' then all RD data bytes transferred after 'RD length byte' data bytes are undefined values. If 'RD length byte' is greater than 'WR length byte' then all WR data bytes transferred after 'WR length byte' data bytes are ignored.

Protocol synchronization is done using /SSEL and SCK. If SCK is high while /SSEL is high, the protocol state is set to idle.

Note: Protocol synchronization is optional and can be omitted as long as no errors have occurred.

**HDR byte 3: errors (in previous data transfer)**

Bit 0 is set if SPI Protocol synchronization interrupted the previous data transfer.

Bit 1 is set if a write buffer overflow occurred in the previous data transfer.

Bit 2 is set if a read buffer underrun occurred in the previous data transfer.

Bit 3 is set if there was an access to an invalid address in the previous data transfer.

**Since the FPGA needs a certain amount of time to boot, the  $\mu$ C should either wait or send a query until the FPGA no longer answers with an error.**

**The FPGA also needs a certain amount of time to connect with the VARAN bus after successful initialization.**

## Recommended Shielding for VARAN

The real-time VARAN Ethernet bus system exhibits very robust characteristics in industrial environments. Through the use of IEEE 802.3 standard Ethernet physics, the potentials between an Ethernet line and sending/receiving components are separated. Messages to a bus participant are immediately repeated by the VARAN Manager in the event of an error. The shielding described below is principally recommended.

For applications in which the bus is run outside the control cabinet, the correct shielding is required. Especially when for structural reasons, the bus line must be placed next to strong electromagnetic interference. It is recommended to avoid placing Varan bus lines parallel to power cables whenever possible.

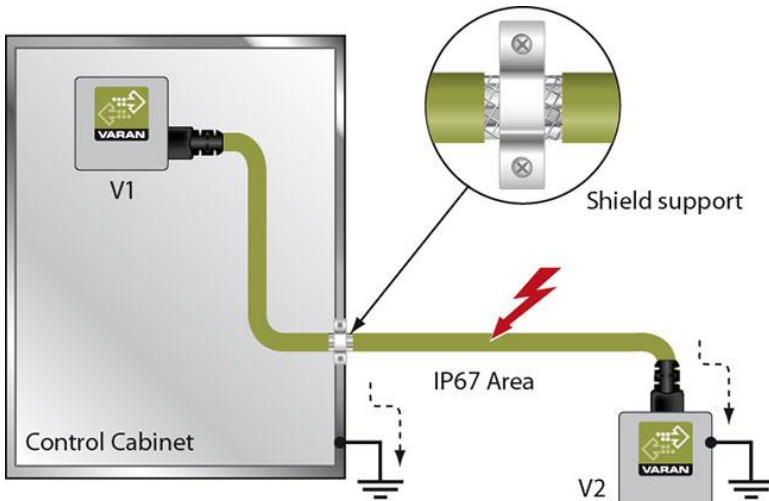
SIGMATEK recommends the use of CAT5e industrial Ethernet bus cables.

For the shielding, an S-FTP cable should be used. An S-FTP bus is a symmetric, multi-wire cable with unshielded pairs. For the total shielding, a combination of foil and braiding is used. A non-laminated variant is recommended.

**The VARAN cable must be secured at a distance of 20 cm from the connector for protection against vibration!**

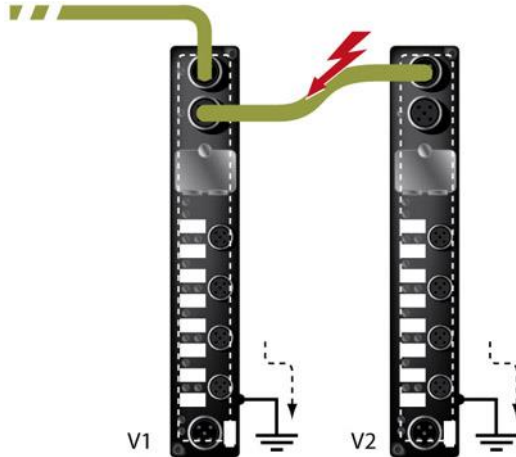
## 1. Wiring from the Control Cabinet to an External VARAN Component

If the Ethernet lines are connected from a VARAN component to a VARAN node located outside the control cabinet, the shielding should be placed at the entry point to the control cabinet housing. All noise can then be dissipated before reaching the electronic components.



## 2. Wiring Outside of the Control Cabinet

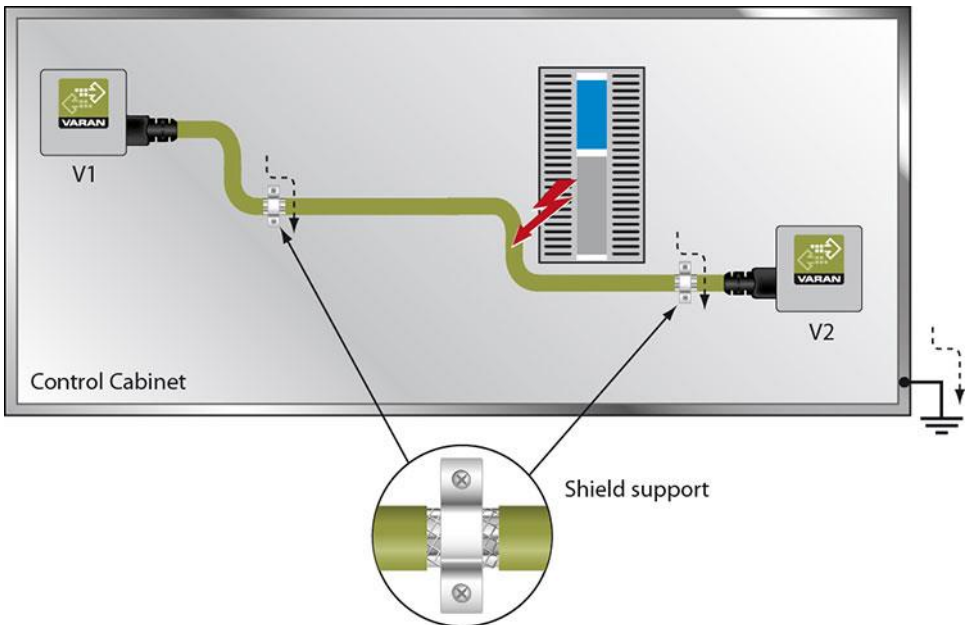
If a VARAN bus cable must be placed outside of the control cabinet only, no additional shield connection is required. This requires that only IP67 modules and connectors be used. These components are very robust and noise resistant. The shielding for all sockets in IP67 modules are internally connected to common bus or electrically connected to the housing, whereby the deflection of voltage spikes does not flow through the electronics.





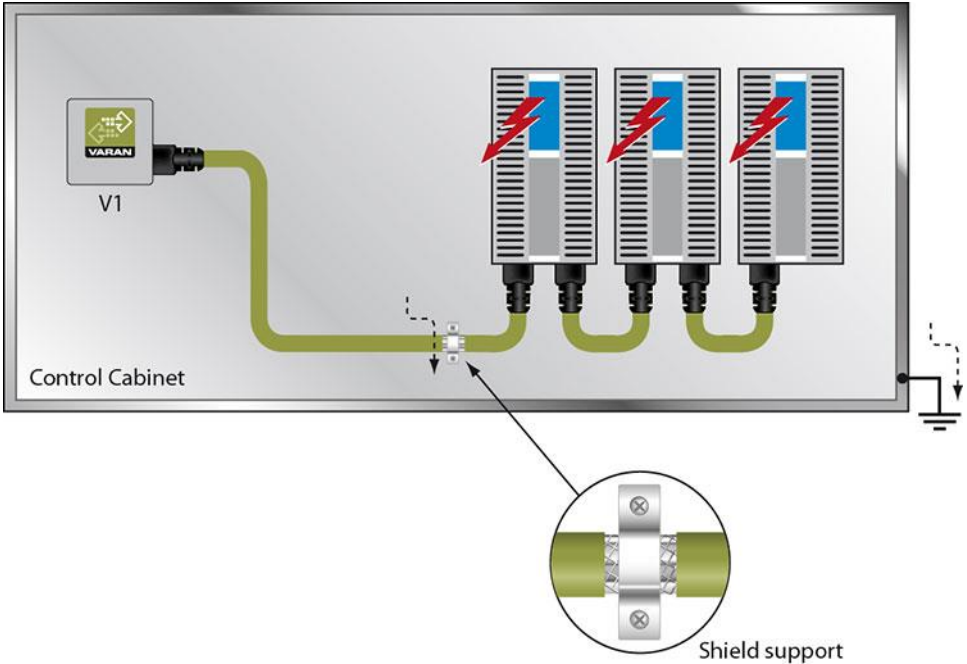
### 3. Shielding for Wiring Within the Control Cabinet

Sources of strong electromagnetic noise located within the control cabinet (drives, Transformers, etc.) can induce interference in a VARAN bus line. Voltage spikes are dissipated over the metallic housing of a RJ45 connector. Noise is conducted over the control cabinet without additional measures needed on the circuit board of electronic components. To avoid error sources with data exchange, it is recommended that shielding be placed before any electronic components in the control cabinet.



## 4. Connecting Noise-Generating Components

When connecting power lines to the bus that generate strong electromagnetic noise, the correct shielding is also important. The shielding should be placed before a power element (or group of power elements).



## 5. Shielding Between Two Control Cabinets

If two control cabinets must be connected over a VARAN bus, it is recommended that the shielding be located at the entry points of each cabinet. Noise is therefore prevented from reaching the electronic components in both cabinets.

