VARAN Client Board VEB 011/012

Versatile **A**utomation **R**andom **A**ccess **N**etwork

This client board provides a simple method of connecting any periphery modules to the VARAN bus.

Technical Data

Performance Data

Internal memory	Serial 4-MBit-Flash
Interfacing	1 x VARAN (Client) (maximum length: 100 m) 1 x Periphery interface
Connection to periphery module	Over 50-pin. Board-to-Board- connector plug, 0,8 mm spacing (Type ERNI Microstac, order no.: 114713)

Electrical Requirements

Internal supply voltage (VDD)	Typically +3,3 V DC (±4 %) (Supplied by the periphery module over the 50-pin connector plug)
Current consumption of the voltage supply	Minimum 250 mA (Depending on the external circuit)

Miscellaneous

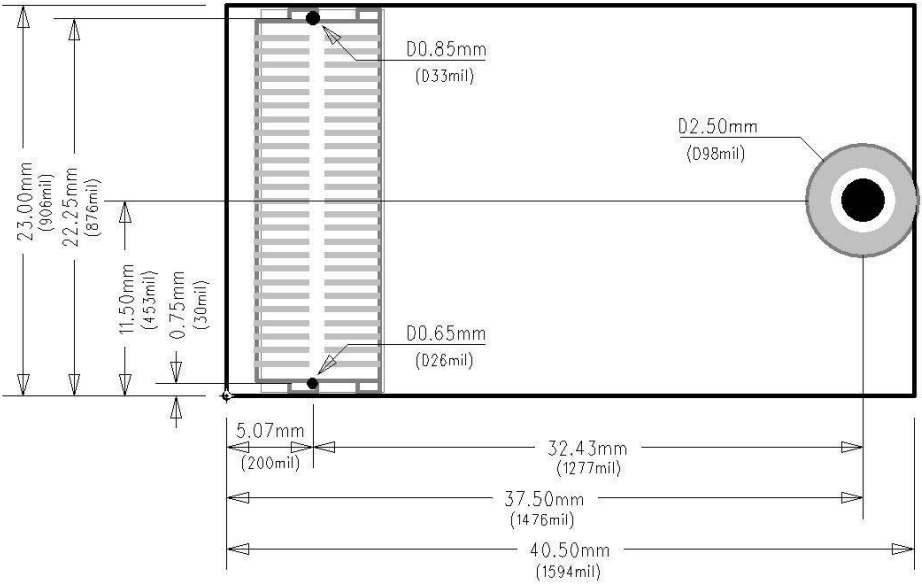
	VEB 011	VEB 012
Article number	16-081-011	16-081-012
Hardware version	1.x	1.x

Environmental Conditions

Storage temperature	-20 – +85 °C	
Operating temperature [1]	VEB 011	VEB 012
	0 – 70 °C	0 – 85 °C
	VEB 011/012	
Humidity	0 – 95 %, uncondensed	
EMV stability	[2]	
Shock resistance	EN 60068-2-27	150 m/s²

[1] The operating temperature of the entire unit must be defined individually for each application since the operating conditions (mounting position, housing, and heat source in the vicinity of the module) are not known.
[2] The EMV stability has to be tested separately in the complete system for each application.

Mechanical Dimensions

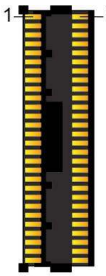


The dimensioning of the center holes of the 50-pole ERNI Board-to-Board connector is effective for the plugs on the base board (doesn't show the position of the connectors on the VEB).

The VEB is shown from the connector back side in this illustration.

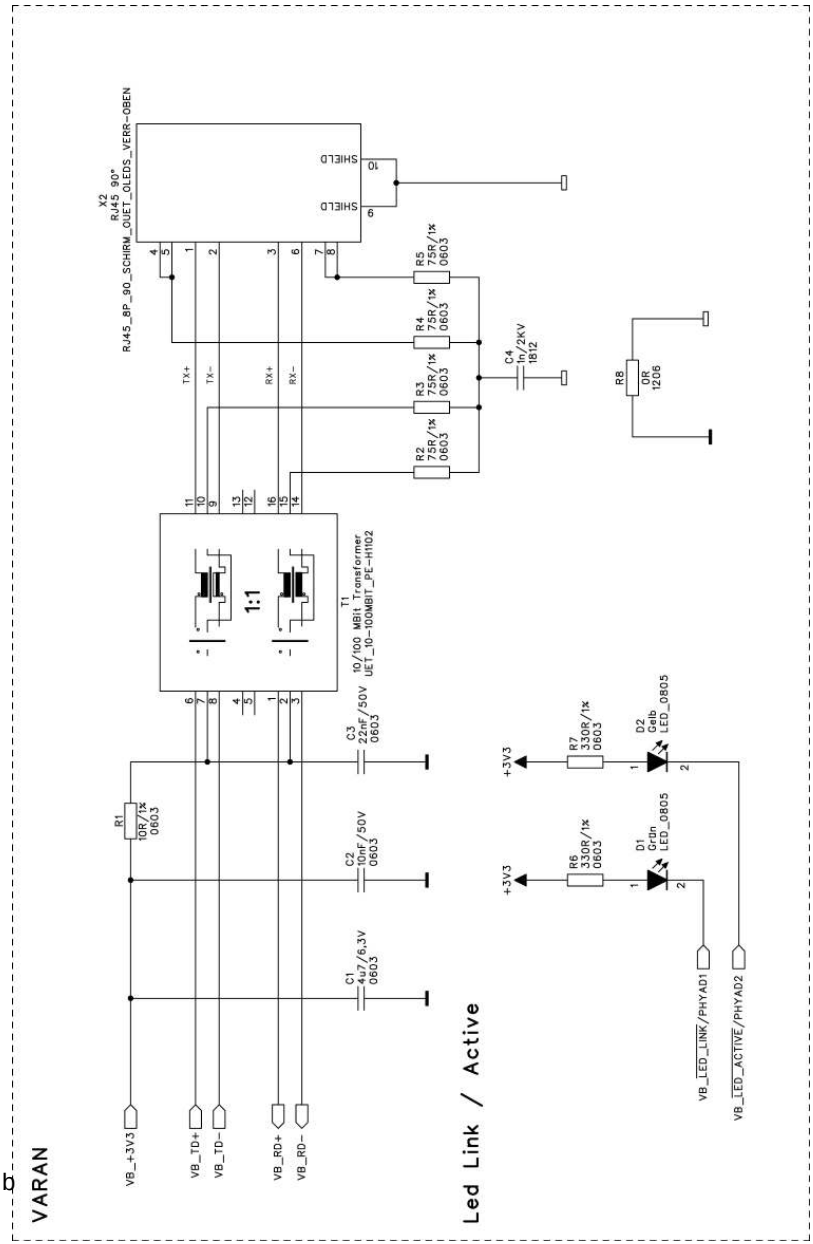
The height of the component parts on the base board under the VEB must not exceed 3 mm.

Connector Layout



Pin	Xilinx Identifier	Bus Mode		DPRAM Mode		IO Mode	
1		GND		GND		GND	
2		GND		GND		GND	
3	V2	D0	IO	D0	IO	IN9	IN
4	V1	-		-		OUT9	OUT
5	V4	D1	IO	D1	IO	IN10	IN
6	V3	-		-		OUT10	OUT
7	V6	D2	IO	D2	IO	IN11	IN
8	V5	-		-		OUT11	OUT
9	V8	D3	IO	D3	IO	IN12	IN
10	V7	-		-		OUT12	OUT
11	V10	D4	IO	D4	IO	IN13	IN
12	V9	-		-		OUT13	OUT
13	V12	D5	IO	D5	IO	IN14	IN
14	V11	Mode0	IN	Mode0	IN	Mode0	IN
15	V14	D6	IO	D6	IO	IN15	IN
16	V13	Mode1	IN	Mode1	IN	Mode1	IN
17	V16	D7	IO	D7	IO	IN16	IN
18	V15	Mode2	IN	Mode2	IN	Mode2	IN
19		VDD		VDD		VDD	
20		VDD		VDD		VDD	
21		GND		GND		GND	
22	V17	Ready	IN	-		-	
23		Phy_RX+		Phy_RX+		Phy_RX+	
24	V18	Sync	OUT	Sync	OUT	-	
25		Phy_RX-		Phy_RX-		Phy_RX-	
26	V19	A0	OUT	A0	OUT	IN1	IN
27		Phy_TX+		Phy_TX+		Phy_TX+	
28	V20	A1	OUT	A1	OUT	IN2	IN
29		Phy_TX-		Phy_TX-		Phy_TX-	
30	V21	A2	OUT	A2	OUT	IN3	IN
31		VB +3V3		VB +3V3		VB +3V3	
32	V22	A3	OUT	A3	OUT	IN4	IN
33	V24	CLK 25 MHz	OUT	CLK 25 MHz	OUT	CLK 25 MHz	OUT
34	V23	A4	OUT	A4	OUT	IN5	IN
35	V26	/Periphery Reset	OUT	/Periphery Reset	OUT	/Periphery Reset	OUT
36	V25	A5	OUT	A5	OUT	IN6	IN
37	V28	-		-		-	
38	V27	A6	OUT	A6	OUT	IN7	IN
39	V30	R / W	OUT	R / W	OUT	OUT8	OUT
40	V29	A7	OUT	A7	OUT	IN8	IN
41	V32	-		-		OUT6	OUT
42	V31	A8	OUT	A8	OUT	OUT7	OUT
43		/Phy_led_link		/Phy_led_link		/Phy_led_link	
44	V33	A9	OUT	A9	OUT	OUT5	OUT
45		/Phy_led_active		/Phy_led_active		/Phy_led_active	
46	V34	A10	OUT	A10	OUT	OUT4	OUT
47	V36	/CS Hex Switch		/CS Hex Switch		OUT2	OUT
48	V35	A11	OUT	A11	OUT	OUT3	OUT
49		GND		GND		GND	
50	V37	/CS	OUT	/CS	OUT	OUT1	OUT

Electrical bonding



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Layout guidelines

- Place blocking capacitors with 100 nF to the supply pins (+3V3) of the Board-to-Board connectors.
- The distance between the transformer (Pulse H1102NLT) and the RJ45 plug connector has to be kept to a minimum (<25 mm)
- The distance between the transformer and the 50-pole VEB plug should not exceed 50mm, if possible.
- The VARAN differential lines TD+/TD- and RD+/RD- are
  - as short as possible
  - parallel
  - of same length
  - … to route
- Furthermore differential lines should have the following properties:
  - Distance between two differential line pairs >0,38 mm
  - Distance of the differential lines to the circuit board angles >25 mm
  - Distance of the differential lines to other signals >0,76 mm
  - Continuous GND area under the differential lines
  - Do not cross differential lines with other signals
  - Do not route differential lines under components

Mode Register

The mode pins (v11, v13, v15) are latched in the FPGA and the selected mode can be read out from the register. Following modes are defined:

V15	V13	V11	Mode
0	0	0	“000” Bus Mode
0	0	1	“001” IO Mode
0	1	0	“010” DPRAM Mode

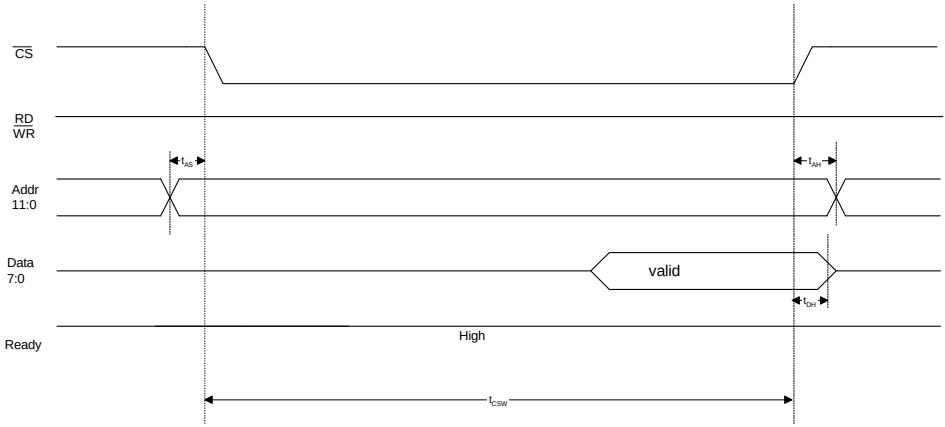
Bus Mode

In the Bus mode the VEB 011 is the bus master. The Sync signal is the output of the PLL (sync out 0) – see VARAN Bus specification. This signal can be used for synchronisation of the periphery.

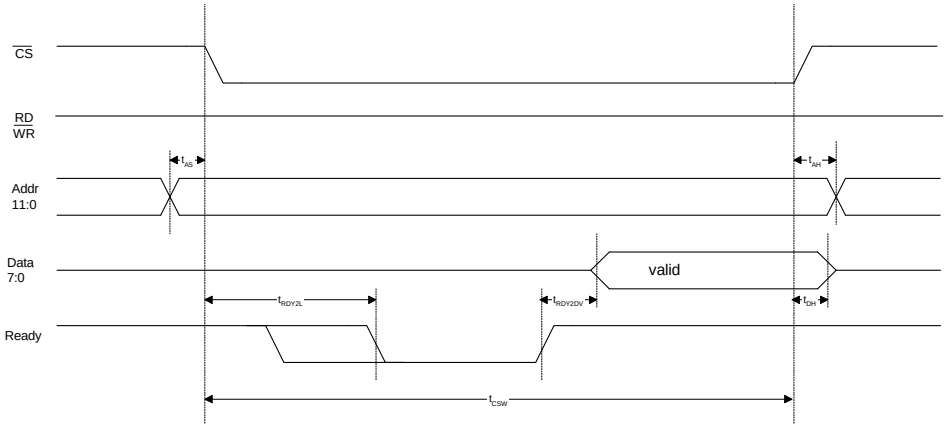
Name	Description	Port	Pins (0 to ..)
A	Address (12 bit)	out	V19, 20, 21, 22, 23, 25, 27, 29, 31, 33, 34, 35
D	Data (8 bit)	inout	V2, 4, 6, 8, 10, 12, 14, 16
R/$\overline{W}$	Read/$\overline{Write}$	out	V30
$\overline{CS}$	$\overline{Chip\ select}$	out	V37
Sync	Sync	out	V18
Ready	Ready	in	V17

Timing Diagram

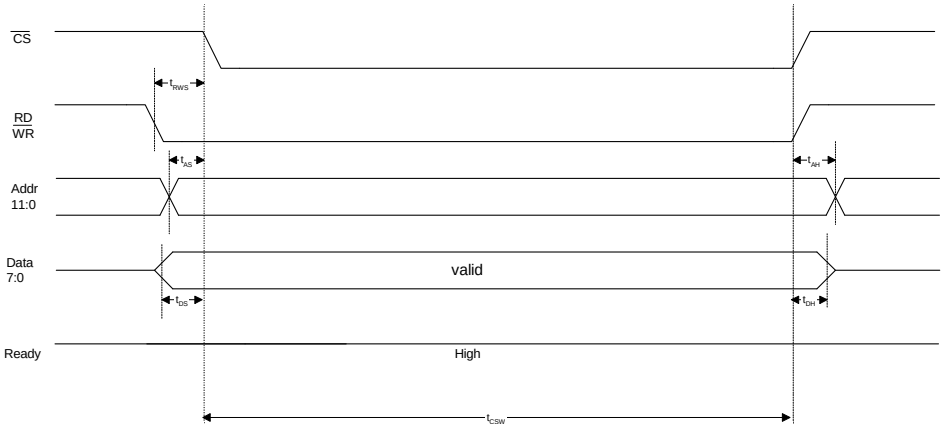
Read (without wait states)



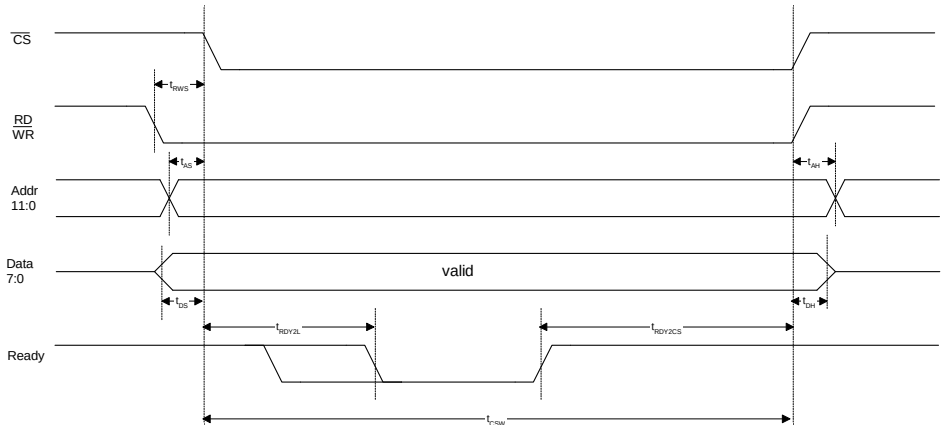
Read (with wait states)



Write (without wait states)



Write (with wait states)



Timing Characteristics

Timing	Time (ns)		Description
	min.	max.	
t_{CSW}	220	-	Chip select low width
t_{RWS}	5	-	Read write setup time
t_{AS}	5	-	Address setup time
t_{DS}	5	-	Data setup time
t_{DH}	0	-	Data hold time
t_{AH}	5	-	Address hold time
t_{RDY2L}	120	-	Chip select to ready low time
t_{RDY2DV}	-	5	Ready to data valid time
t_{RDY2CS}	60	-	Ready to chip select

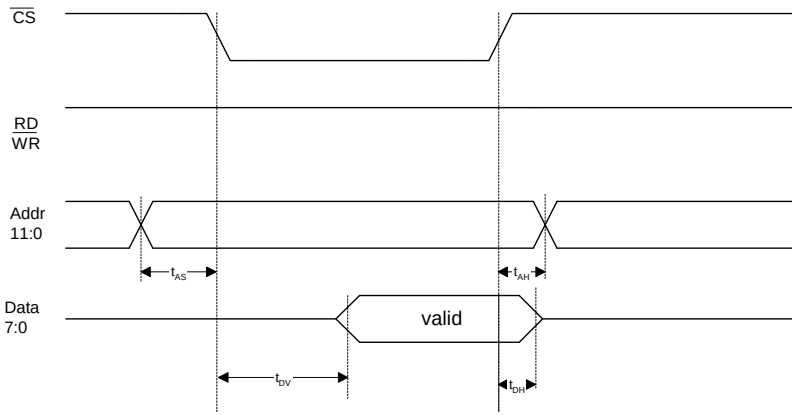
DPRAM Mode

In the DPRAM mode the VEB 011 is the bus client. An external bus master can access the DPRAM in the FPGA. The DPRAM is organized in 4096 x 8 bits on both sides. The Sync signal is the output of the PLL (sync out 0) – see VARAN Bus specification. This signal can be used for synchronisation of the periphery.

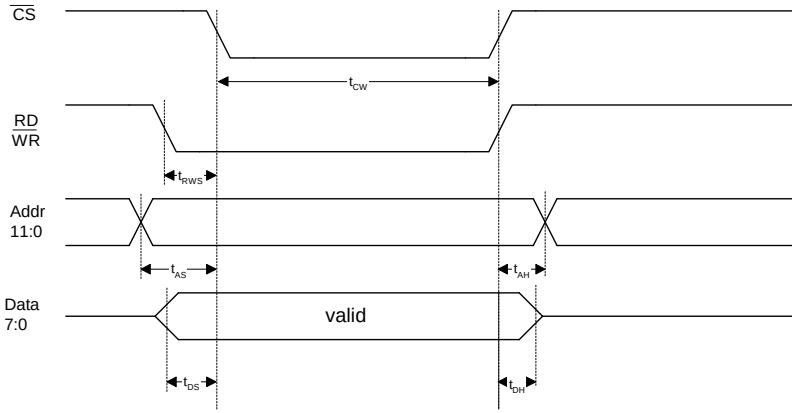
Name	Description	Port	Pins (0 to ..)
A	Address (12 bit)	in	V19, 20, 21, 22, 23, 25, 27, 29, 31, 33, 34, 35
D	Data (8 bit)	inout	V2, 4, 6, 8, 10, 12, 14, 16
R/$\overline{W}$	Read/$\overline{Write}$	in	V30
$\overline{CS}$	$\overline{Chip\ select}$	in	V37
Sync	Sync	out	V18

Timing Diagram

Read



Write



Timing Characteristics

Timing	Time (ns)		Description
	min.	max.	
t_{CW}	55	-	Chip select to end of write
t_{RWS}	0	-	Read write setup time
t_{AS}	0	-	Address setup time
t_{DS}	0	-	Data setup time
t_{DH}	0	-	Data hold time
t_{AH}	0	-	Address hold time
t_{DV}	-	70	Chip select to data valid time

Read Hex Switch

After switch-on the FPGA reads in the hex switches in Bus Mode and DPRAM Mode. During this process the periphery remains in reset.

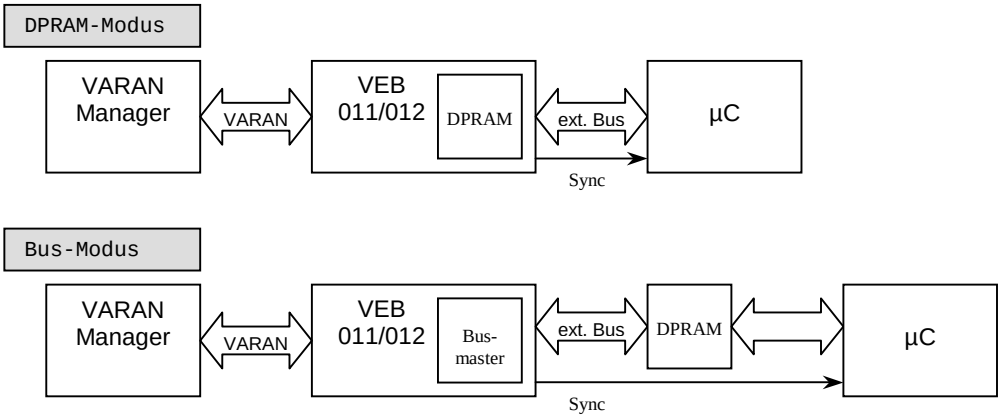
The read hex switches are stored in the varan configuration register.

Name	Description	Port	Pins (0 to ..)
Hex Switch	Hex Switch (8 bit)	inout	V2, 4, 6, 8, 10, 12, 14, 16
$\overline{CS}$	$\overline{Chip\ select}$	out	V36

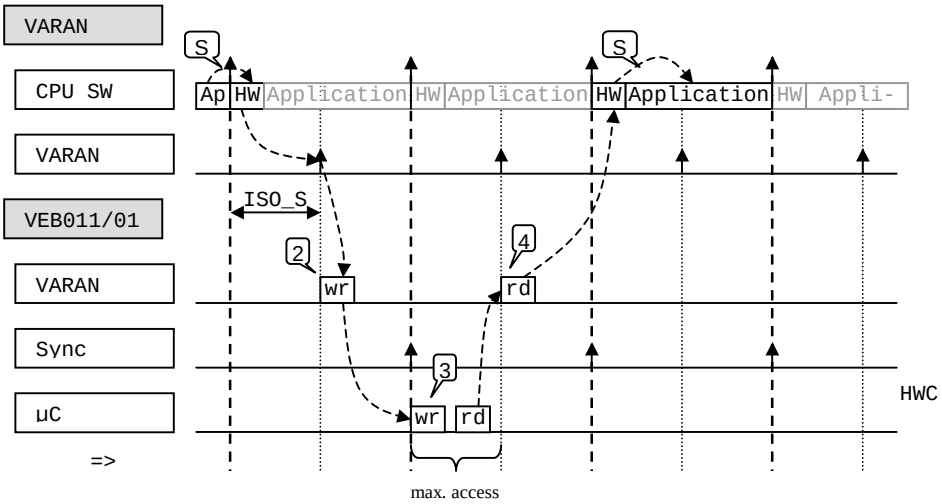
VEB 011/012 Time response

A DPRAM gives a microcomputer the option of exchanging data with the VARAN system. For this, the VEB 011/012 provides two variations, one that uses the FPGA internal DPRAM and another for an external DPRAM. So that data consistency in the 4-kbyte DPRAM is ensured, the microcomputer must be synchronized with the VARAN bus and can only exchange data in the allowed time window. The Sync signal gives the microcomputer permission to access the DPRAM. The data exchange must then be completed within half the VARAN system time to avoid generating inconsistent data.

Block Diagram



Time diagram



Hardware Class

SW => Software
wr => Write
rd => Read
ISO_S => ISO Start point (adjustable from 10 – 90 %)

Zeitliches Verhalten am VEB011/012

1	HW Class writes to DO RAM	
2	VARAN writes to DPRAM	500 µs (half Cycle@1ms Cycle time)
3	µC writes and reads DPRAM	
4	VARAN read from DPRAM	500 µs (half Cycle@1ms Cycle time)
5	HW Class reads from DO RAM	

Addressing

Address (hex)	Size (Byte)	Access type	Description	Reset value
Memory				
0000	528	-	Reserved	
0210	1	r	VEB011 Mode Register Bit 0 .. 2: Mode Bit 3 .. 7: Reserved "000" Bus mode "001" IO mode "010" DPRAM mode	00
0211	15	-	Reserved	
0220	1	w	Digital Out Register Bit 0: OUT1 Bit 1: OUT2 Bit 2: OUT3 Bit 3: OUT4 Bit 4: OUT5 Bit 5: OUT6 Bit 6: OUT7 Bit 7: OUT8 (Access only allowed in IO mode)	00
0220	1	r	Digital Input Register Bit 0: IN1 Bit 1: IN2 Bit 2: IN3 Bit 3: IN4 Bit 4: IN5 Bit 5: IN6 Bit 6: IN7 Bit 7: IN8 (Access only allowed in IO mode)	
0221	1	w	Digital Out Register Bit 0: OUT9 Bit 1: OUT10 Bit 2: OUT11 Bit 3: OUT12 Bit 4: OUT13 Bit 5 .. 7: Reserved (Access only allowed in IO mode)	00
0221	1	r	Digital Input Register Bit 0: IN9 Bit 1: IN10 Bit 2: IN11 Bit 3: IN12 Bit 4: IN13 Bit 5: IN14 Bit 6: IN15 Bit 7: IN16 (Access only allowed in IO mode)	

0222	3550	-	Reserved	
1000	4096	r/w	Bus Master (Access only allowed in Bus mode) Note: These registers have a slower processing time of the VARAN client. t_{client} = 230 ns + 300 ns/byte (see VARAN Bus timing in the VARAN Bus specification)	
2000	4096	r/w	DPRAM (Access only allowed in DPRAM mode)	

More information on the VARAN bus can be found in the VARAN bus specifications!

VARAN Recommended Shielding

The VARAN real-time Ethernet bus system offers robust performance in harsh industrial environments. Through the use of IEEE 802.3 standard Ethernet physics, the potential between an Ethernet line and sending/receiving components is kept separate. The VARAN Manager resends messages to a bus participant immediately when an error occurs. It is principally recommended that the shielding guidelines below be followed.

For applications in which the bus line is run outside the control cabinet, correct shielding is required. This is especially important, if due to physical requirements, the bus lines must be placed next to sources of strong electromagnetic noise. It is recommended that whenever possible, to avoid wiring VARAN-Bus lines parallel to power cables.

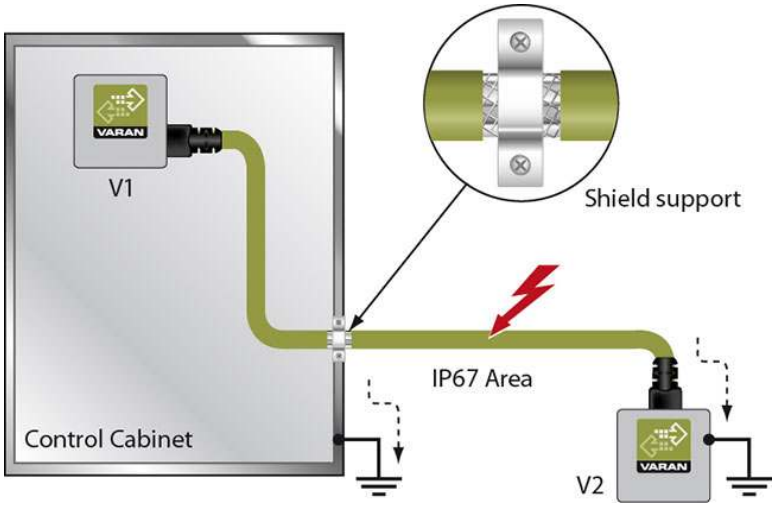
SIGMATEK recommends the use of **CAT5e** industrial Ethernet bus lines.

For the shielding variants, an S-FTP bus line is recommended, which is a symmetric, multi-wire cable with unshielded pairs. For the total shielding, a combination of foil and braiding is used; it is recommended that an unvarnished variant be used.

The VARAN cable must be secured at a distance of 20 cm from the connector for protection against vibration!

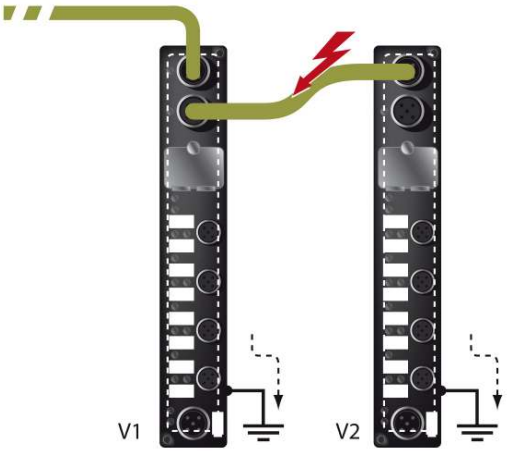
1. Wiring from the Control Cabinet to an External VARAN Component

If the Ethernet lines are connected from a VARAN component to a VARAN node outside the control cabinet, the shielding should be placed at the entry point to the control cabinet housing. All noise can then be deflected from the electronic components before reaching the module.



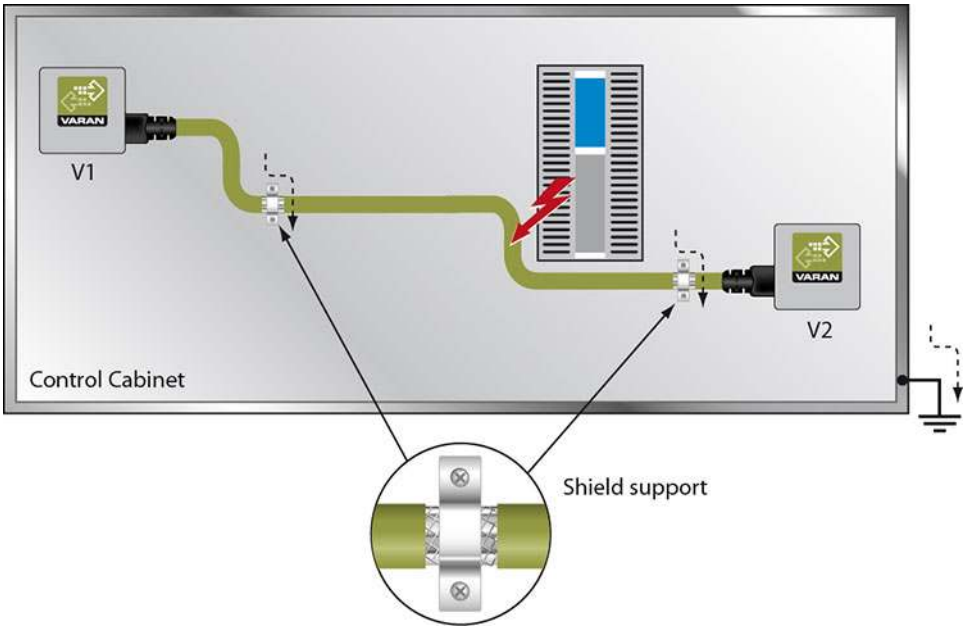
2. Wiring Outside of the Control Cabinet

If a VARAN bus cable must be placed outside of the control cabinet only, no additional shield connection is required. This requires that only IP67 modules and connectors be used. These components are very robust and noise resistant. The shielding for all sockets in IP67 modules are internally connected to common bus or electrically connected to the housing, whereby the deflection of voltage spikes does not flow through the electronics.



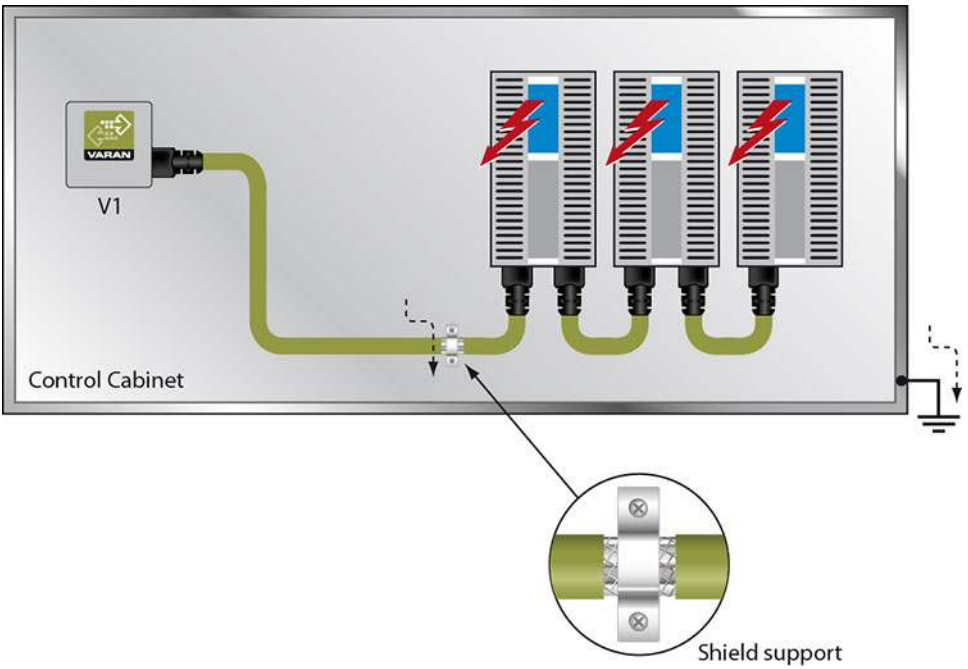
3. Shielding for Wiring Within the Control Cabinet

Sources of strong electromagnetic noise located within the control cabinet (drives, Transformers, etc.) can induce interference in a VARAN bus line. Spike voltages are deflected over the metallic housing of a RJ45 connector. Noise is conducted through the control cabinet housing without further action from the electronic components To eliminate sources of noise during data transfer, it is recommended that the shielding from all electronic components be connected within the control cabinet.



4. Connecting Noise-Generating Components

With the connection of power components that generate strong electromagnetic noise, it is also critical to ensure correct shielding. The shielding should be placed before a power component (or a group thereof).



5. Shielding Between Two Control Cabinets

If two control cabinets must be connected over a VARAN bus, it is recommended that the shielding be located at the entry points to both cabinets. Noise can thereby be kept from reaching the electronics within the control cabinet.