SIGMATEK

IO 011S

S-DIAS Smart Multi I/O Module

Instruction Manual

Date of creation: 04.05.2018 | Version date: 26.07.2023 | Article number: 20-013-011S-DE

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Translation of the Original Instructions

S-DIAS Smart Multi I/O Module IO 011S

with 6 digital inputs

8 digital back-readable short-circuit proof outputs

1 analog voltage input

1 analog current input

The module has 6 digital inputs (+24 V/3.5 mA/1 µs) and 8 short-circuit proof digital, back-readable outputs (+24 V/0.5 A/150 µs).

The digital inputs and back-reading of the digital outputs have a latch mode with which, based on the CPU cycle, a timestamp in µs is generated with the rising/falling/both edges of the input or back-read. The digital outputs have a time-trigger mode with which, based on the CPU cycle, the outputs can be set at a specific time offset in µs.

The voltage supply for the digital outputs are monitored for under voltage.

Additionally, the module has an analog ±10 V/16-bit/100 kHz voltage and a 0-20 mA/16-bit/1 kHz current input.

The analog inputs have a latch mode with which, based on the CPU cycle, a timestamp in µs is generated with the rising/falling/both edges when the upper/lower limits of a configurable voltage/current are exceeded. The analog inputs also have a time-trigger mode with which, based on the CPU cycle, the inputs can be read.

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1 Introduction

1.1 Target Group/Purpose of this Operating Manual

This operating manual contains all information required for the operation of the product.

This operating manual is intended for:

- Project planners
- Technicians
- Commissioning engineers
- Machine operators
- Maintenance/test technicians

General knowledge of automation technology is required.

Further help and training information, as well as the appropriate accessories can be found on our website www.sigmatek-automation.com.

Our support team is happily available to answer your questions.
Please see our website for our hotline number and business hours.

1.2 Important Reference Documentation

This and additional documents can be downloaded from our website or obtained through support.

1.3 Contents of Delivery

1x IO 011S

2 Basic Safety Directives

2.1 Symbols Used

The following symbols are used in the operator documentation for warning and danger messages, as well as informational notes:

DANGER

Danger indicates that death or serious injury **will occur**, if the specified measures are not taken.

⇨ To avoid death or serious injuries, observe all guidelines.

Danger indique une situation dangereuse qui, faute de prendre les mesures adéquates, **entraînera** des blessures graves, voire mortelles.

⇨ Respectez toutes les consignes pour éviter des blessures graves, voire mortelles.

WARNING

Warning indicates that death or serious injury **can** occur, if the specified measures are not taken.

⇨ To avoid death or serious injuries, observe all guidelines.

Avertissement d'une situation dangereuse qui, faute de prendre les mesures adéquates, **entraînera** des blessures graves, voire mortelles.

⇨ Respectez toutes les consignes pour éviter des blessures graves, voire mortelles.

CAUTION

Caution indicates that moderate to slight injury **can** occur, if the specified measures are not taken.

⇨ To avoid moderate to slight injuries, observe all guidelines.

Attention indique une situation dangereuse qui, faute de prendre les mesures adéquates, **peut** entraîner des blessures assez graves ou légères.

⇨ Respectez toutes les consignes pour éviter des blessures graves, voire mortelles.

INFORMATION

Information

⇨ Provides important information on the product, handling or relevant sections of the documentation, which require attention.

2.2 Disclaimer

INFORMATION

The contents of this operating manual were prepared with the greatest care. However, deviations cannot be ruled out. This operating manual is regularly checked and required corrections are included in the subsequent versions. The machine manufacturer is responsible for the proper assembly, as well as device configuration. The machine operator is responsible for safe handling, as well as proper operation.

The current operating manual can be found on our website. If necessary, contact our support.

Subject to technical changes, which improve the performance of the devices. The following operating manual is purely a product description. It does not guarantee properties under the warranty.

Please thoroughly read the corresponding documents and this operating manual before handling a product.

SIGMATEK GmbH & Co KG is not liable for damages caused through, non-compliance with these instructions or applicable regulations.

2.3 General Safety Directives

The Safety Directives in the other sections of this operating manual must be observed. These instructions are visually emphasized by symbols.

INFORMATION

According to EU Directives, the operating manual is a component of a product.

This operating manual must therefore be accessible in the vicinity of the machine since it contains important instructions.

This operating manual should be included in the sale, rental or transfer of the product, or its online availability indicated.

Regarding the requirements for Safety and health connected to the use of machines, the manufacturer must perform a risk assessment in accordance with machine directives 2006/42/EG before introducing a machine to the market.

Operate the unit with devices and accessories approved by SIGMATEK only.

CAUTION

Handle the device with care and do not drop or let fall.

Prevent foreign bodies and fluids from entering the device.

The device must not be opened!

Manipulez l'appareil avec précaution et ne le laissez pas tomber.

Empêchez les corps étrangers et les liquides de pénétrer dans l'appareil.

L'appareil ne doit pas être ouvert!

If the device does not function as intended or has damage that could pose a danger, it must be replaced!

En cas de fonctionnement non conforme ou de dommages pouvant entraîner des risques, l'appareil doit être remplacé!

The module complies with EN 61131-2.

In combination with a facility, the system integrator must comply with EN 60204-1 standards.

For your own safety and that of others, compliance with the environmental conditions is essential.

Le module est conforme à la norme EN 61131-2.

En combinaison avec une équipement, l'intégrateur de système doit respecter la norme EN 60204-1.

Pour votre propre sécurité et celle des autres, le respect des conditions environnementales est essential.

2.4 Software/Training

The application is created with the software LASAL CLASS 2 and LASAL SCREEN Editor.

Training for the LASAL development environment, with which the product can be configured, is provided. Information on our training schedule can be found on our website.

3 Standards and Directives

3.1 Directives

The product was constructed in compliance with the following European Union directives and tested for conformity.

3.1.1 EU Conformity Declaration

EU Declaration of Conformity

The product IO 011S conforms to the following European directives:

- **2014/35/EU** Low-voltage Directive
- **2014/30/EU** Electromagnetic Compatibility (EMC Directive)
- **2011/65/EU** “Restricted use of certain hazardous substances in electrical and electronic equipment” (RoHS Directive)

The EU Conformity Declarations are provided on the SIGMATEK website. See Products/Downloads or use the search function and the keyword “EU Declaration of Conformity”.

4 Type Plate

Exemplary nameplate (symbol image)

HW: Hardware version
SW: Software version

5 Technical Data

5.1 Digital Input Specifications

Number	6	
Input voltage	typically +24 V	maximum +30 V
Signal level	low: < +8 V	high: > +14 V
Switching threshold	typically +11 V	
Input current	3.7 mA at +24 V	
Latch mode timestamp	0 to (32767 - bus cycle time) in 1 µs increments	
Input delay	typically 1 µs	

5.2 Digital Back-Readable Output Specifications

Number	8	
Short-circuit proof	yes	
Maximum permissible continuous load current/channel	0.5 A	
Maximum total current (all 8 outputs)	4 A (100% of on-time)	
Maximum output braking energy (inductive load)	maximum 1 Joule/channel	
Residual current output (off)	≤ 10 µA	
Hardware enable delay(1)	< 100 µs	
Hardware enable delay (1)	< 150 µs	
Time-trigger mode time offset	0 to (32767 - bus cycle time) in 1 µs increments	
Back-read signal level	low: < +8 V	high: > +14 V
Input delay	typically 1 µs	
Latch mode timestamp	0 to (32767 - bus cycle time) in 1 µs increments	
Maximum allowed voltage on the digital output when switched off	An external voltage supplied to the digital output pin must not exceed the voltage on the supply pin (24 V) by more than 0.7 V.	

(1) This involves a maximum value for the turn-on delay (output voltage above 90% of the supply voltage) and turn-off delay (output voltage below 10% of the supply voltage) at a 24 V, 0.5 A ohmic load and 25 °C ambient temperature. The actual turn-on or turn-off delay is dependent on the supply voltage, load and temperature. In addition, due to their tolerances, the times can vary from component to component.

5.3 Voltage Monitor

Power supply +24 V	Supply voltage > 18 V (DC OK-LED lights green)

5.4 ±10 V Analog Input Specifications

Number of channels	1	
Measurement range	-10 ... +10 V	0 ... +10 V
Measurement value	-30.000 … +30.000	0 … +30.000
	With an open input, the firmware returns the positive maximum value and a status bit to indicate a cable break (HW class shows the value -2147483632)	
Input type	differential input	
Resolution	16 Bit (ca. 0.3 mV/LSB)	
Conversion time per channel	default mode: 10 µs (current input disabled) default mode: 20 µs (current input enabled) Time-trigger mode: 15 µs (current input disabled/enabled) latch mode: 10 µs (current input disabled, 1-4 latch registers enabled) latch mode: 20 µs (current input disabled, 5-8 latch registers enabled) latch mode: 20 µs (current input enabled, 1-8 latch registers enabled)	
Minimum bus cycle time for PDO data exchange	1 ms	
Latch mode upper and lower threshold preset value	-30.000 … +30.000	0 … +30.000
Latch mode timestamp	0 to (32767 - bus cycle time) in 1 µs increments	
Time-Trigger mode time offset	0 to (32767 - bus cycle time) in 1 µs increments	
Common mode range	±12 V	
Input resistance	typically 660 kΩ	
Cable break monitor	yes	
Input filter hardware	typically 100 kHz, low pass 3rd order	
Input filter software	configurable low pass 1st order system (in standard mode only)	
Noise	±8d (without software filter)	
Base accuracy incl. calibration errors, linearity and noise at 25 °C	±0.20 % of maximum measurement value	
Temperature drift 0-60 °C	±0.10 % of maximum measurement value	
Total accuracy (0-60 °C)	±0.30 % of maximum measurement value	

5.5 Analog Current Input Specifications

Number of channels	1	
Measurement range	0-20 mA	4-20 mA
Measurement value	0-60,000	12,000-60,000
		With an open input, the firmware returns the positive maximum value and a status bit to indicate a cable break (HW class shows the value -2147483632)
Input type	difference input	
Resolution	16 Bit (ca. 0.3 µA/LSB)	
Conversion time per channel	default mode: 10 µs (voltage input disabled) default mode: 20 µs (voltage input enabled) Time-trigger mode: 15 µs (voltage input disabled/enabled) latch mode: 10 µs (voltage input disabled, 1-4 latch register enabled) latch mode: 20 µs (voltage input disabled, 5-8 latch register enabled) latch mode: 20 µs (voltage input enabled, 1-8 latch register enabled)	
Minimum bus cycle time for PDO data exchange	1 ms	
Latch mode upper and lower threshold preset value	0-60,000	12,000-60,000
Latch mode timestamp	0 to (32767 - bus cycle time) in 1 µs increments	
Time-trigger mode time offset	0 to (32767 - bus cycle time) in 1 µs increments	
Common mode range	±10 V	
Input resistance	typically 50Ω	
Cable break monitor	no	yes, can be set from 0 - 4 mA via software (default: 3 mA)
Short circuit monitoring	no	yes, can be set from 0 - 4 mA via software (default: 3 mA)
Input filter hardware	typically 1 kHz, low pass 3rd order	
Input filter software	configurable low pass 1st order system (in standard mode only)	
Noise	±7d (without software filter)	
Base accuracy incl. calibration errors, linearity and noise at 25 °C	±0.30 % of maximum measurement value	
Temperature drift 0-60 °C	±0.20 % of maximum measurement value	
Total accuracy (0-60 °C)	±0.50 % of maximum measurement value	

5.6 Electrical Requirements

Power supply +24 V	18-30 V DC [1]	
Current consumption of +24 V power supply	corresponds to the load on the digital outputs	
Voltage supply from S-DIAS bus	+5 V	
Current consumption on the S-DIAS bus (+5 V power supply)	typically 70 mA	maximum 75 mA
Voltage supply from S-DIAS bus	+24 V	
Current consumption on the S-DIAS bus (+24 V power supply)	typically 20 mA	maximum 25 mA
UL-Standard	For UL[1] : must be powered with SELV/PELV and limited energy	

[1] Designed in the USA in accordance with Class 2 UL 508 for use with a Class 2 transformer or power source. The secondary circuit is rated according to the requirements of UL 508, section 63.29 with exception of No. 1 of section 32.4.4 or 32.5.1. The insulation and rating of the overcurrent protection require installation with limited voltage / current

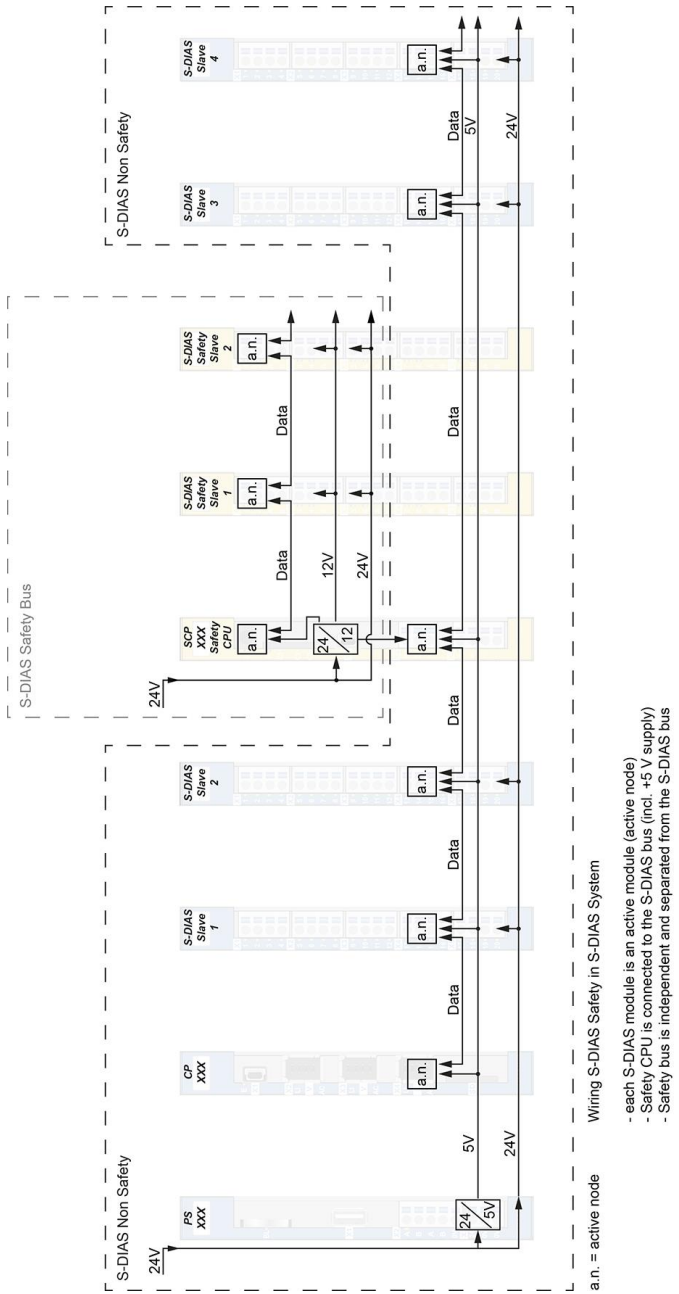
INFORMATION

If this S-DIAS module is connected to an S-DIAS supply module with several S-DIAS modules, the total current of the modules used must be determined and checked.

The total current of the +24 V supply cannot exceed 1.6 A!

The total current of the +5 V supply cannot exceed 1.6 A!

The specification for the current can be found in the module-specific documentation under "Electrical Requirements".


S-DIAS Non Safety
S-DIAS Safety Bus
S-DIAS Non Safety
24V
PS XXX
CP XXX
S-DIAS Slave 1
S-DIAS Slave 2
SCP XXX Safety CPU
S-DIAS Safety Slave 1
S-DIAS Safety Slave 2
S-DIAS Slave 3
S-DIAS Slave 4
a.n.
Data
5V
12V
24V
24/5
24/12
a.n. = active node
Wiring S-DIAS Safety in S-DIAS System
- each S-DIAS module is an active module (active node)
- Safety CPU is connected to the S-DIAS bus (incl. +5 V supply)
- Safety bus is independent and separated from the S-DIAS bus

5.7 Miscellaneous

Article number	20-013-011S
Standard	UL 508 (E247993) in preparation
Approvals	cUL, CE, UKCA

5.8 Environmental Conditions

Storage temperature	-20 ... +85 °C	
Environmental temperature	0 ... +60 °C	
Humidity	0-95 %, non-condensing	
Installation altitude above sea level	0-2000 m without derating > 2000 m up to a maximum of 5000 m with derating of the maximum environmental temperature by 0.5 °C per 100 m	
Operating conditions	pollution degree 2	
EMC resistance	in accordance with EN 61000-6-2 (industrial area)	
EMC noise generation	in accordance with EN 61000-6-4 (industrial area)	
Vibration resistance	EN 60068-2-6	3.5 mm from 5-8.4 Hz 1 g from 8.4-150 Hz
Shock resistance	EN 60068-2-27	15 g
Protection type	EN 60529	IP20

5.9 S-DIAS Protocol Version

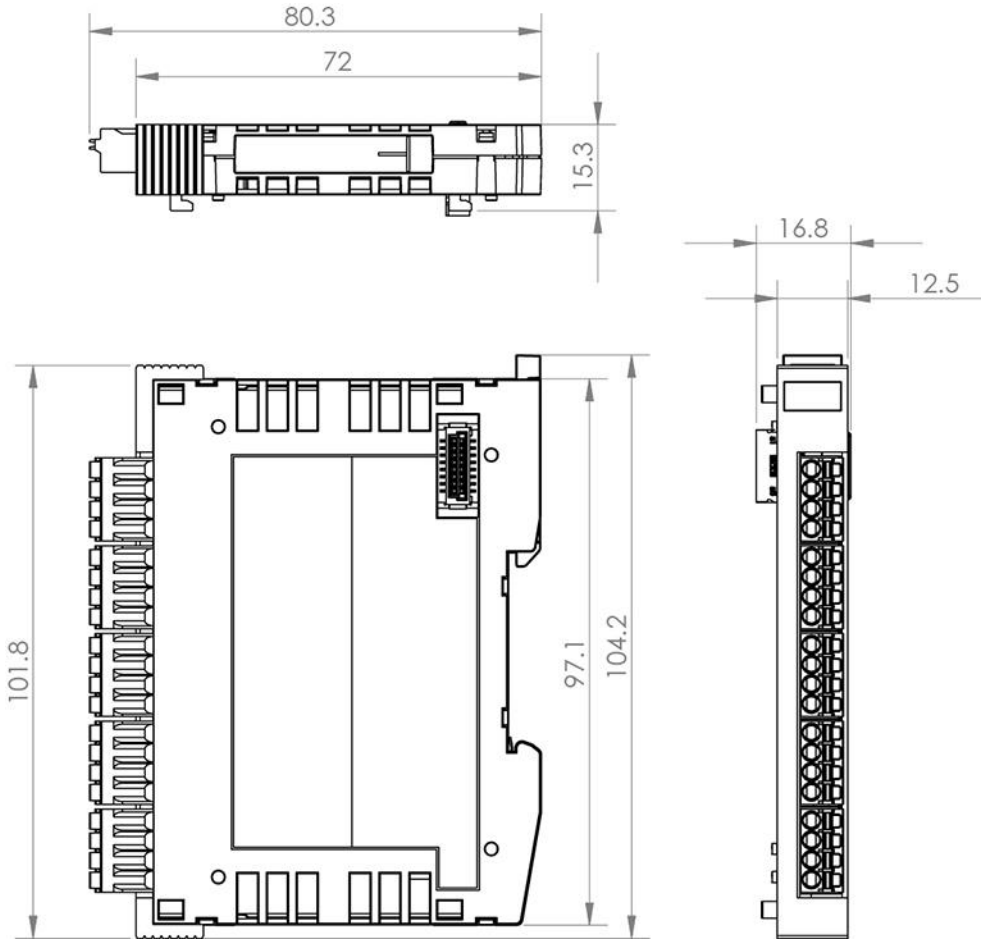
For a correct function of the IO 011S, a S-DIAS protocol version v1.3.0 must be supported by the Master/Manager CPU. This is the case with:

- CP 101 since FPGA version v1.2
- CP 102 since FPGA version v1.2
- CP 111 since FPGA version v1.4
- CP 112 since FPGA version v1.3
- CP 212 since FPGA version v1.4
- CP 311 since FPGA version v1.4
- CP 312 since FPGA version v1.3
- CP 731 since FPGA version v1.0

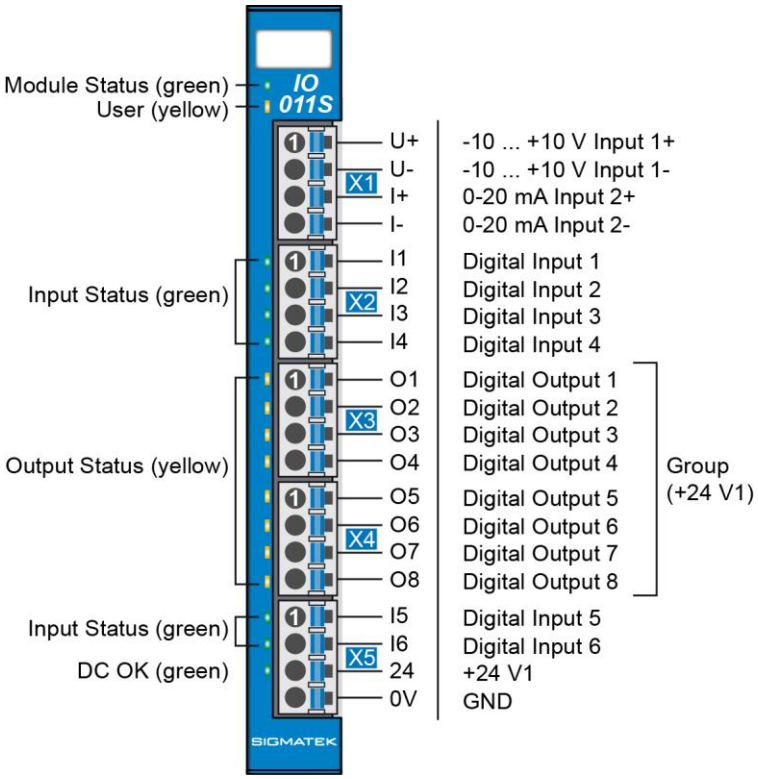
INFORMATION

The S-DIAS protocol version 1.3.0 requires an operating system-version higher than 09.02.50/09.03.112.

6 Mechanical Dimensions



7 Connector Layout



7.1 Status LEDs

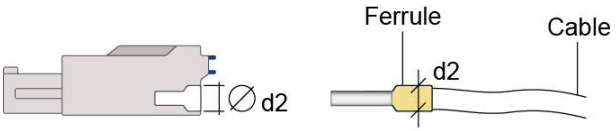
Module Status	green	ON	module active
		OFF	no supply available
		BLINKING (5 Hz)	no communication
User	yellow	ON	can be set from the application (e.g. the module LED can be set to blinking through the visualization, so that it is easily found in the control cabinet)
		OFF	
		BLINKING (2 Hz)	
		BLINKING (4 Hz)	
Input Status	green	ON	input ON
		OFF	input OFF
Output Status	yellow	ON	output ON
		OFF	output OFF
DC OK	green	ON	voltage is supplied to the output group

7.2 Applicable Connectors

Connectors:
X1-X5: Connectors with spring terminals (included in delivery)
The spring terminals are suitable for the connection of ultrasonically compressed (ultrasonically welded) strands.

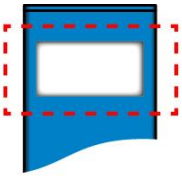
Connections:

Stripping length/sleeve length:	10 mm
Mating direction:	parallel to the conductor axis or circuit board
Conductor cross section rigid:	0.2-1.5 mm^2
Conductor cross section flexible:	0.2-1.5 mm^2
Conductor cross-section strands ultrasonically compacted:	0.2-1.5 mm^2
Conductor cross section AWG/kcmil:	24-16
Conductor cross section flexible with ferrule without plastic sleeve:	0.25-1.5 mm^2
Conductor cross section flexible with ferrule with plastic sleeve:	0.25-0.75 mm^2 (reason for reduction d2 of the ferrule)



d2 = max. 2.8 mm

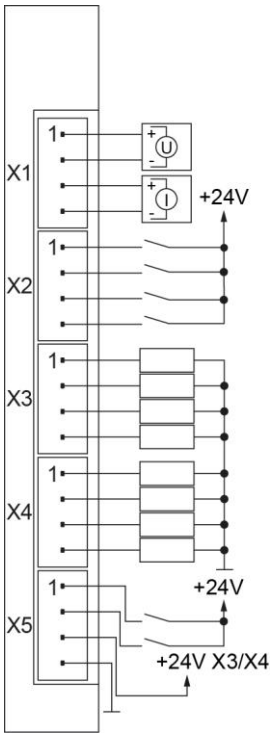
7.3 Label Field



Manufacturer	Weidmüller
Type	MF 10/5 CABUR MC NE WS
Article number Weidmüller	1854510000
Compatible printer	Weidmüller
Type	Printjet Advanced 230V
Article number Weidmüller	1324380000

8 Wiring

8.1 Wiring Example



8.2 Guidelines for Digital Outputs

The fast digital inputs have a minimal input filter to provide a high time resolution. Due to the minimal input filtering, the inputs are more sensitive to noise than standard digital inputs. It is therefore recommended that the signal lines be shielded. The shield must be placed as close as possible to the module.

8.3 Guidelines for Digital Outputs

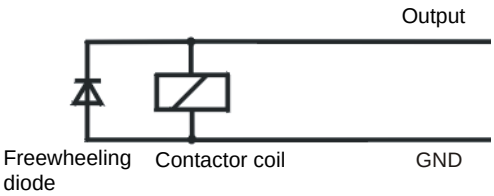
- Up to 8 outputs are powered by a common +24 V supply.
- The cross section of the conductor for the +24 supply must be sufficient for the maximum total current.
- The outputs and can be turned off by turning off the +24 V supply voltage.
- Applying power to an output whose supply voltage exceeds 0.7 V is not allowed.
- For applications with high temporal precision of the output signal's rising and falling edges in the microsecond range, it is recommended that the signal lines be shielded from EMV noise. The shield must be placed as close as possible to the module.

INFORMATION

Inductive loads must always be connected to a freewheeling diode or an RC network. This should be placed as close to the load as possible.

The S-DIAS module CANNOT be connected/disconnected while voltage is applied!

8.3.1 Connecting Inductive Loads



8.4 Guidelines for Analog Inputs

The signals recorded by the analog modules are very small in comparison to the digital signals. To ensure error-free operation, a careful wiring method must be followed:

The DIN rail must have an adequate mass connection.

The lines connected to the source of the analog signals must be as short as possible and parallel wiring to digital signal lines must be avoided.

The signal lines must be shielded.

The shielding must be connected to a shielding bus.

Avoid parallel connections between input lines and load-bearing circuits.

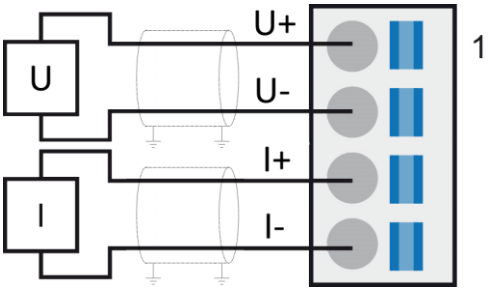
Protective circuits for all relays (RC networks or free-wheeling diodes).

INFORMATION

Connect the ground bus to the control cabinet.

The S-DIAS module CANNOT be connected/disconnected while voltage is applied!

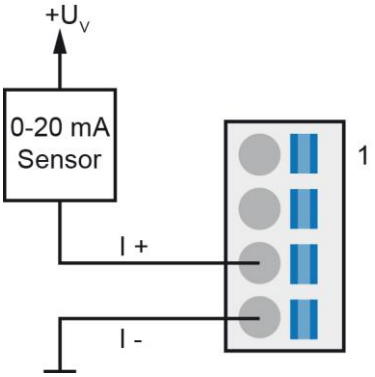
8.5 Connection of the Signal Source



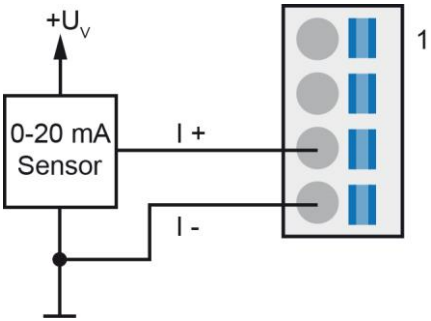
INFORMATION

The common mode range of ±10 V must be obtained for each signal pin.

8.6 Connecting a 2-Wire Sensor



8.7 Connecting a 3-wire sensor



9 Assembly/Installation

9.1 Check Contents of Delivery

Ensure that the contents of the delivery are complete and intact. See chapter 1.3 Contents of Delivery.

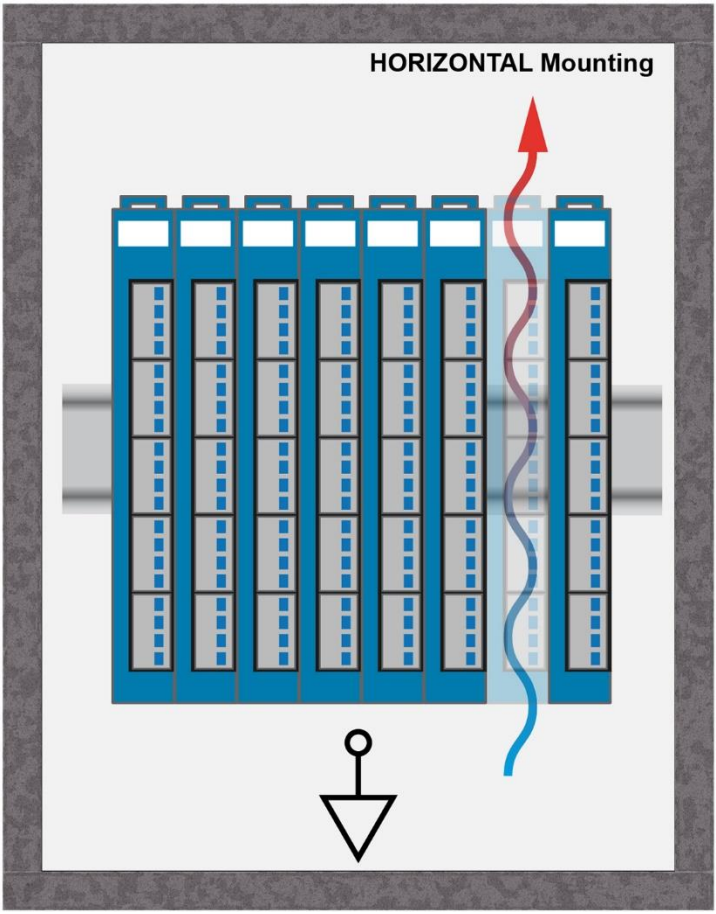
INFORMATION

On receipt and before initial use, check the device for damage. If the device is damaged, contact our customer service and do not install the device in your system.

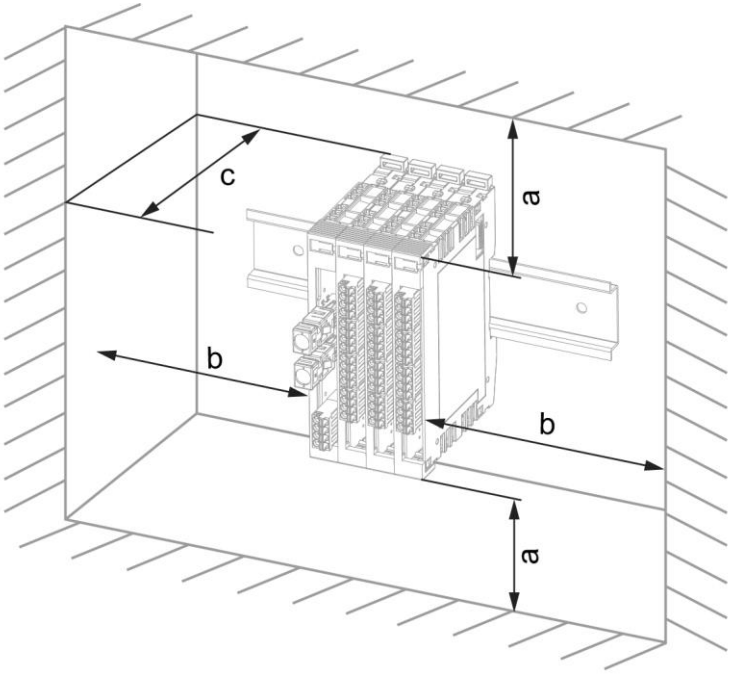
Damaged components can disrupt or damage the system.

9.2 Mounting

The S-DIAS modules are designed for installation into the control cabinet. To mount the modules, a DIN-rail is required. The DIN rail must establish a conductive connection with the back wall of the control cabinet. The individual S-DIAS modules are mounted on the DIN rail as a block and secured with latches. The functional ground connection from the module to the DIN rail is made via the grounding clamp on the back of the S-DIAS modules. The modules must be mounted horizontally (module label facing up) with sufficient clearance between the ventilation slots of the S-DIAS module blocks and nearby components and/or the control cabinet wall. This is necessary for optimal cooling and air circulation, so that proper function up to the maximum operating temperature is ensured.



Recommended minimum distances of the S-DIAS modules to the surrounding components or control cabinet wall:



a	b	c
30 mm (1.18″)	**30 mm** (1.18″)	**100 mm** (3.94″)

a, b, c … distances in mm (inches)

10 Digital Input/Back-Reading Output Operating Modes

The digital inputs and back-reading of the digital outputs can be operated in either Standard or latch mode. In latch mode, up to 128 registers can be assigned to the individual inputs.

10.1 Standard Mode

In the standard mode, the status of the input and digital output back-reading is transmitted to the hardware class during each cycle.

10.2 Latch Mode

In latch mode, up to 128 registers for time measurement including edge definition, are assigned to the individual digital inputs or read-backs of the digital outputs. If multiple registers are assigned to an input or back-reading, a FIFO process is generated. The time to the first edge is written to the first assigned register, the time to the second edge to the second assigned register, etc. If at an input or while back-reading, more edges have been detected in the cycle than registers configured for the input or back-read, an overflow bit is set for the affected input or back-read. If none of the selected edges were detected, a Null-Info bit is set for the affected input or back-read. All unused registers receive the same value as the last register used for the input.

The latch function can be set to rising, falling or both edges.

11 Digital Output Operating Modes

The digital outputs can be operated in either Standard or time-trigger mode. To define the time offset and the condition to set, 8x8 registers are available that can be distributed over the outputs as desired.

11.1 Standard Mode

In Standard mode, the outputs are set each cycle via the defined values in the hardware class.

11.2 Time-Trigger Mode

In the time-trigger mode, the status of the digital outputs can be changed at a defined time between two cycles. The time for changing the output status and the status to set are specified by the HW class in the cyclic data for each output. The time between status changes, must be at least as long as the turn-on/off time of the output.

12 Analog Input Operating Modes

The analog inputs of the IO 011S can be operated in either Standard mode, time-trigger mode or latch mode. This can be configured via bits 2 and 3 in the Info byte of the configuration data. 8x2 registers each are available to preset threshold values for the latch mode and 8 registers for presetting time-trigger values. These 8 registers or register pairs can be distributed between both inputs as desired (e.g.: 2 for the voltage input, 6 for the current input or all 8 for the voltage input).

12.1 Standard Mode

In this mode, the analog inputs are scanned as fast as possible and filtered to achieve the highest possible sampling rate. The time point of the individual measurements cannot be defined since measuring is continuous.

12.2 Time-Trigger Mode

In the time-trigger mode, the analog inputs are measured only once per internal cycle. The HW class specifies the time point of the measurement process for each analog input in the cyclic data for the firmware. The reference time in µs, managed by the HW class, is distributed to all S-DIAS modules.

The adjustable time-trigger points are subject to the following limits:

The time-trigger points take effect in the following cycle: The time-trigger values must be cyclically transferred from the hardware class to the firmware. These are however, only take effect in the following internal cycle, since the firmware must first test and activate the values.

Time-trigger value: The time-trigger value is defined in µs intervals with 15-bit values, based on the actual reference time given by the HW class.

Output value: The time-trigger value set in the internal cycle n is first enabled in the cycle n+1. The measured value can then be output in cycle n+2. The HW class reads this value at the beginning of cycle n+3.

Interval between the time-trigger points: Since it is not possible to measure multiple analog inputs simultaneously, the interval between offsets must be at least 15 µs.

Correction within the firmware: If time-triggers are set values too close together, they are corrected (shifted) by the firmware wherever possible. If a correction is made, a “time-trigger corrected” bit is set for the control (HW class).

12.3 Latch Mode

In latch mode, the control provides 8x2 latch registers with preset values that can be assigned to the inputs as desired. To generate a Schmitt-trigger response, one register each is available for the upper and lower value. The inputs are scanned as fast as in standard mode and each new value is checked as to whether it meets the defined condition. Possible conditions are:

Rising edge: The new value is above/equal to the upper threshold value and the lower threshold was previously exceeded.

Falling edge: The new value is below/equal to the lower threshold value and the upper threshold was previously exceeded.

Both edges: Evaluation of the rising and falling edges.

The current time stamp is written in the latch register with the first configured edge only. Here, a flag is set to ignore the following edges. If no edges are detected in a cycle, the corresponding bit in the Null-Info register remains at 1 (this is then reset by writing to the PDO).

12.3.1 Note

Due to the internal noise of the module, signal jitter can be generated during evaluation in latch mode if the difference between the upper and lower threshold is 0. With cyclic signals, the time stamp can deviate slightly. The signal jitter depends on the slew rate and noise from the input signal.

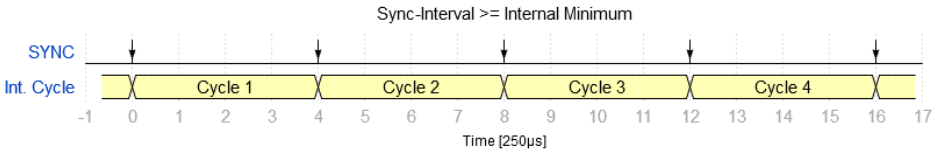
13 Synchronization with the Master CPU

Since the minimum processing time of cyclic data is limited, but multiple sync/cycle times must be supported, there are various internal cycle times (ICT) depending on the S-DIAS Sync Interval (SDSI):

13.1 SDSI is Above/Equal to the Minimum ICT

The SDSI is assumed as the ICT directly.

Example:

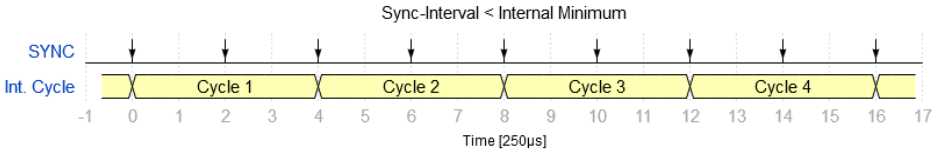


Here, a sync interval of 1 ms is used. The minimum internal cyclic time is for example, 500 µs. An internal cyclic time of 1 ms results.

13.2 SDSI is Below the Minimum ICT

The ICT is set to the next divisible interval via the SDSI (based on the interval minimum).

Example:



Here, a sync interval of 500 µs is used. This time, the minimum internal cyclic time is 1 ms. For this reason, only every second sync is used as the main sync. The intermediate sync is used to continue synchronization when the main sync fails. The synchronization for the sync is performed once power ICT.

14 Addressing

14.1 FPGA – HW Class Addressing

Digital in and outputs are operated by the FPGA of the IO 011S directly. Whereby, a section of the address area is therefore required. This area is not used by the firmware.

Address (hex)	Size (bytes)	Access Type	Description
0000	**192**	**w**	**Cyclic Data for Firmware / CPLD**
0000	1	w	Output register Bit 0: output 1 Bit 1: output 2 … Bit 7: Output 8
0001	1	w	Null-Info Register Bit 0: output 1 Bit 1: output 2 … Bit 7: Output 8
0002	2	w16	Offset output register 1 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
0004	2	w16	Offset output register 2 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
0006	2	w16	Offset output register 3 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
0008	2	w16	Offset output register 4 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
000A	2	w16	Offset output register 5 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
000C	2	w16	Offset output register 6 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
000E	2	w16	Offset output register 7 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
0010	2	w16	Offset output register 8 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)

0012	2	w16	Offset output register 8 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
...	...	w16	Offset output register n Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
0080	2	w16	Offset output register 64 (output X) Bit 14..0: Time offset in 1 µs Bit 15: Output value, which is set (low/high)
00C0	**320**	**r**	**Cyclic Data for the HW class**
00C0	2	r16	Input register Bit 0: input 1 Bit 1: input 2 … Bit 5: Input 6 Bit 6: DIAG back-reading Bit 7: DC 24 V OK Bit 8: Backreading output 1 Bit 9: Backreading output 2 … Bit 15: Backreading output 8
00C2	2	r16	Null-Info Register Bit 0: input 1 Bit 1: input 2 … Bit 5: Input 6 Bit 6: DIAG back-reading Bit 7: DC 24 V OK Bit 8: Backreading output 1 Bit 9: Backreading output 2 … Bit 15: Backreading output 8
00C4	2	r16	Overflow register Bit 0: input 1 Bit 1: input 2 … Bit 5: Input 6 Bit 6: DIAG back-reading Bit 7: DC 24 V OK Bit 8: Backreading output 1 Bit 9: Backreading output 2 … Bit 15: Backreading output 8
00C6	2	r16	Latch register 1 (input X) Bit 15: Edge indicator (1 = rising, 0 = falling) Bit14..0: Timestamp in 1 µs resolution

00C8	2	r16	Latch register 2 (input X) Bit 15: Edge indicator (1 = rising, 0 = falling) Bit14..0: Timestamp in 1 µs resolution
...	...	r16	Latch register n Bit 15: Edge indicator (1 = rising, 0 = falling) Bit14..0: Timestamp in 1 µs resolution
01C4	2	r16	Latch register 128 (back-read output X) Bit 15: Edge indicator (1 = rising, 0 = falling) Bit14..0: Timestamp in 1 µs resolution
0200	**128**	**w**	**Configuration Data for CPLD**
0200	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for input 1 Bit 6: 1 = Latch enable for rising edge input 1 Bit 7: 1 = Latch enable for falling edge input 1
...			
0205	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for input 6 Bit 6: 1 = Latch enable for rising edge input 6 Bit 7: 1 = Latch enable for falling edge input 6
0206	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for input Diag back-reading Bit 6: 1 = Latch enable for rising edge Diag back-reading Bit 7: 1 = Latch enable for falling edge Diag back-reading
0207	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for DC 24 V OK Bit 6: 1 = Latch enable for rising edge DC 24 V OK Bit 7: 1 = Latch enable for falling edge DC 24 V OK
0208	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for input back-reading output 1 Bit 6: 1 = Latch enable for rising edge back-reading output 1 Bit 7: 1 = Latch enable for falling edge back-reading output 1
...			
020F	1	r/w	Edge definition/distribution of the register for input latch[1)] Bit 5..0: Number of latch registers for input back-reading output 8 Bit 6: 1 = Latch enable for rising edge back-reading output 8 Bit 7: 1 = Latch enable for falling edge back-reading output 8
0210	1	r/w	Distribution of the offset output register Bit 5..0: Number of offset output registers for output 1 Bit 7..6: Reserved, write 0, read undefined
...			
0217	1	r/w	Distribution of the offset output register Bit 5..0: Number of offset output registers for output 8 Bit 7..6: Reserved, write 0, read undefined

0218	1	r/w	Output register multiplexer Bit 0: Enable offset output register for output 1 .. Bit 7: Enable offset output register for output 8 (0 = not used, output register is assigned to output, 1= offset output register used, multiple offset output registers can be configured)

14.2 Firmware – HW Class Addressing

Address (hex)	Size (bytes)	Access Type	Description
0000	**192**	**w**	**Cyclic Data for Firmware / CPLD**
0082	2	w	Time-Offset register 1 in µs from sync ⇨ Can be used for AI and AO *(the time offsets are automatically adjusted)*
0084	2	w	Time-Offset register 2
0086	2	w	Time-Offset register 3
0088	2	w	Time-Offset register 4
008A	2	w	Time-Offset register 5
008C	2	w	Time-Offset register 6
008E	2	w	Time-Offset register 7
0090	2	w	Time-Offset register 8

00C0	320	r	Cyclic Data for the HW Class
01C6	2	r	Status Bit 0 24 V DC not OK Bit 1 not synchronized Bit 2 FLASH calibration checksum error Bit 3 FLASH calibration checksum error Bit 4 invalid calibration data Bit 5 S-DIAS cyclic time not supported Bit 6 toggle bit (inverted by the FW with each write process) Module-Specific: Bit 7-8 reserved Bit 9 Data Ready (set to 1 as soon as all analog inputs are stabilized and valid) Other: Bit 10-11 reserved Error information: Bit 12-15 Error codes 00 …….. no errors occurred 01 …….. periphery could not be initialized 02 …….. system clock could not be initialized 03-14 ..... reserved 15 …….. undefined error occurred
01C8	2	r	**Analog input 1 (voltage)** If the default mode is used, the filtered value is output here. In latch mode, the last value measured is output here.
01CA	2	r	**Analog input 2 (current)** If the standard mode is used, the filtered value is output here. In latch mode, the last value measured is output here.

01CC	1	r	**Measurement range testing** (if default mode is active, the AIx measurement range bit applies and when Timeoffset mode is active, the TimeoffsetX bit applies) Bit 0 AI1 or Timeoffset 1 over range Bit 1 AI1 or Timeoffset 1 under range Bit 2 AI2 or Timeoffset 2 over range Bit 3 AI2 or Timeoffset 2 under range Bit 4 Timeoffset 3 over range Bit 5 Timeoffset 3 under range … Bit 14 Timeoffset 8 over range Bit 15 Timeoffset 8 under range
01CE	1	r	**Time Offset Information** Bit 1 Time-Offsets must be corrected *(Selected interval too low)* Bit 2-7 reserved
01CF	1	r	**Null-Info Register** (0 = edge detected, 1 = edge not detected) Bit 0 Time Offset_AI or latch register 1 Bit 1 Time Offset_AI or latch register 2 … Bit 7 Time Offset_AI or latch register 8
01D0	2	r	Time Offset_AI or latch register 1 <u>Mode:</u> **Time-Offset:** The value sampled with Time-Offset 1 is output. If this register is configured for the current input, a constant offset of 1000 is added in the FW to also display the negative values. This offset must then be subtracted when evaluating of the hardware class. (Bit 0-15: AI-value) **Latch:** The time stamp at which the configure edge occurred is output If no edge is detected, the corresponding bit in the Null-Info register is set. Bit 0-14 … time stamp since last Sync in µs Bit 15 … edge: 0 = falling; 1 = rising
01D2	2	r	Time Offset_AI or latch register 2
01D4	2	r	Time Offset_AI or latch register 3

01D6	2	r	Time Offset_AI or latch register 4
01D8	2	r	Time Offset_AI or latch register 5
01DA	2	r	Time Offset_AI or latch register 6
01DC	2	r	Time Offset_AI or latch register 7
0200	**128**	**w**	**Firmware Configuration Data**
0220	2	w	CRC16 over the entire configuration data
0222	2	w	Length of the configuration data
0224	1	w	Info (special purpose or status bits) Bit 0 raw value mode 0 ... normal mode (in and output values compared) 1 ... raw values are used and provided Bit 1 reserved Bit 2-3 ADC – timing mode 0 ... default mode (the ADC is read over a measurement timer as fast as possible) 1 ... time-offset mode (the analog inputs are sampled with the predefined time offsets of the HW class) 2 … latch mode (the inputs are read as fast as possible and when the latch condition is met, the actual time stamp is written to the latch register) Rest → default mode Bit 4-7 reserved
0225	1	w	Message Counter
0226	1	w	Newest protocol version supported
0227	1	w	Current protocol version used
0228	2	w	S-DIAS sync interval in µs
022A	2	w	Start of internal timing in µs (if this instant time point is reached, the FW starts the internal timing. Whereby the FW and hardware class operate synchronously)

022C	2	w	Configuration of the analog inputs Bit 0 analog input 1 0 … -10 V to +10 V 1 ... 0 V to +10 V Bit 1 analog input 2 0 … 0 mA to 20 mA 1 ... X mA to 20 mA (X corresponds to the configured threshold) Bit 4-7 reserved Bit 8 Deactivate analog input 1 (0 … AI1 active; 1 … AI1 deactivated) Bit 9 Deactivate analog input 2 Bit 10-15 reserved
022E	2	w	Analog input 1 frequency limit low pass filter in Hz (with a frequency limit setting of 0 Hz, the software low pass filter is deactivated. Compliance with the sampling theorem must be ensured)
0230	2	w	Analog input 2 frequency limit low pass filter in Hz (For guidelines see address 0x022C)
0232	2	w	Cable-break detection limit AI2 in µA from 0 to 4000. Used when AI2 is configured from “X mA to 20 mA”.

0234	4	w	Distribution of the time offset register over inputs Bit 0-3 input assignment for register 1 0 … no input 1 … analog input 1 2 … analog input 2 3-15 … not allowed (interpreted as “no input”) Bit 4-7 input assignment for register 2 0 … no input … … Bit 28-31 input assignment for register 8 0 … no input … Note: The channels must be sorted in ascending order. Example: Register1 = AI1, Register2 = AI1, Register3 = AI2, Register4 = no AI If the sequence is incorrect, the process stops with the first error. In the following example, register 3 triggers a stop since the sequence is incorrect: Register1 = AI2, Register2 = AI2, Register3 = AI1, Register4 = no AI
0238	4	w	Assignment of the threshold value register to the inputs Same structure as address 0x0232 (these two fields can also be combined if needed)
023C	2	w	Edge definition Bit 0-1 latch register 1 0 = no edge 1 = rising edge 2 = falling edge 3 = both edges Bit 2-3 latch register 2 … Bit 14-15 latch register 8
023E	2	w	Latch 1 – lower threshold value Specified in the same unit in which the corresponding input is otherwise output (mV or µA).
0240	2	w	Latch 1 – upper threshold value Specified in the same unit in which the corresponding input is otherwise output (mV or µA).
0242	2	w	Latch 2 – lower threshold value

0244	2	w	Latch 2 – upper threshold value
0246	2	w	Latch 3 – lower threshold value
0248	2	w	Latch 3 – upper threshold value
024A	2	w	Latch 4 – lower threshold value
024C	2	w	Latch 4 – upper threshold value
024E	2	w	Latch 5 – lower threshold value
0250	2	w	Latch 5 – upper threshold value
0252	2	w	Latch 6 – lower threshold value
0254	2	w	Latch 6 – upper threshold value
0256	2	w	Latch 7 – lower threshold value
0258	2	w	Latch 7 – upper threshold value
025A	2	w	Latch 8 – lower threshold value
025C	2	w	Latch 8 – upper threshold value
0280	**128**	**r**	**HW Class Configuration Data**
0280	2	r	CRC16 over the entire configuration data
0282	2	r	Length of the configuration data
0284	2	r	Firmware version
0286	1	r	Message Counter
0287	1	r	reserved
0288	2	r	Newest protocol version supported
0289	1	r	Current protocol version used
028A	2	r	Internal cyclic time of the FW in µs

15 Supported Cycle Times

15.1 Cycle Times below 1 ms (in µs)

50	100	125	200	250	500
					x

x= supported

15.2 Cycle Times equal to or higher than 1 ms (in ms)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x= supported

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x= supported

16 Transport/Storage

INFORMATION

This device contains sensitive electronics. During transport and storage, high mechanical stress must therefore be avoided.

For storage and transport, the same values for humidity and vibration as for operation must be maintained!

Temperature and humidity fluctuations may occur during transport. Ensure that no moisture condenses in or on the device, by allowing the device to acclimate to the room temperature while turned off.

When sent, the device should be transported in the original packaging if possible. Otherwise, packaging should be selected that sufficiently protects the product from external mechanical influences. Such as cardboard filled with air cushioning.

17 Storage

INFORMATION

When not in use, store the operating panel according to the storage conditions. See chapter 16.

During storage, ensure that all protective covers (if available) are placed correctly, so that no contamination, foreign bodies or fluids enter the device.

18 Maintenance

INFORMATION

During maintenance as well as servicing, observe the safety instructions from chapter 2 Basic Safety Directives.

18.1 Service

This product was constructed for low-maintenance operation.

18.2 Repair

INFORMATION

In the event of a defect/repair, send the device with a detailed error description to the address listed at the beginning of this document.

For transport conditions, see chapter 16 Transport/Storage.

19 Disposal

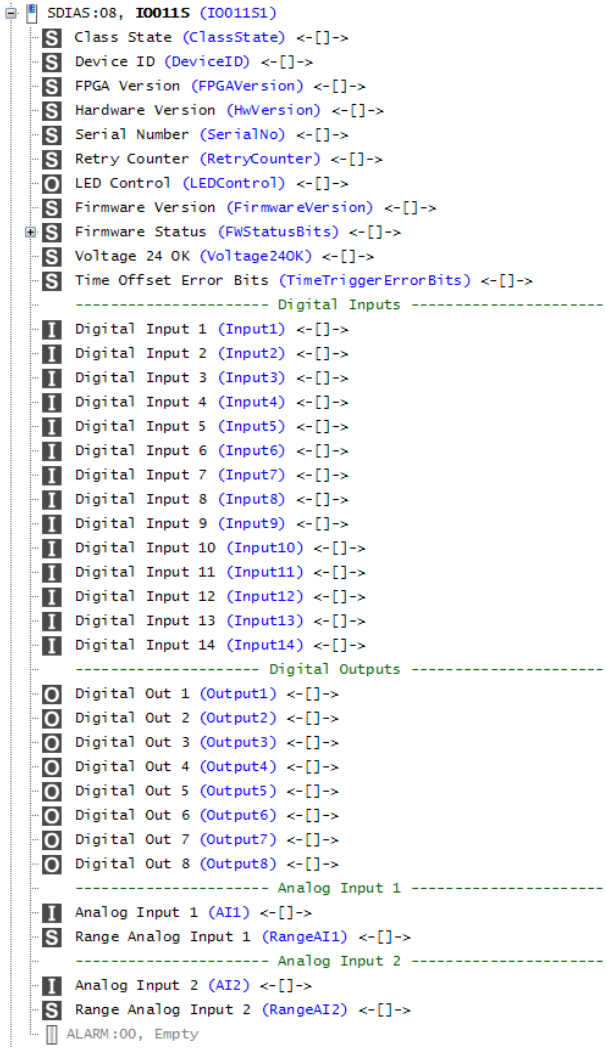
INFORMATION

Should you need to dispose of the device, the national regulations for disposal must be followed.

The device appliance must not be disposed of as household waste.

20 Hardware Class IO011S

IO011S for the S-DIAS multi I/O module IO011S



This hardware class is used to control the RC 001 hardware module. The module has 6 digital inputs and 8 digital outputs (back-readable). In addition, 2 analog inputs are available.
More information on the hardware can be found in the module documentation.

20.1 Interfaces

20.1.1 General

Class State	State	This server shows the actual status of the hardware class.
Device ID	State	The device ID of the hardware module is shown in this server.
FPGA Version	State	FPGA version of the module in 16#XY (e.g. 16#10 = version 1.0).
Hardware Version	State	Hardware version of the module in format 16#XXYY (e.g. 16#0120 = version 1.20)
Serial Number	State	The serial number of the hardware module is shown in this server.
Retry Counter	State	This server increments when a data transfer fails.
LED Control	Output	With this server, the application LED of the S-DIAS module can be activated to find the module in the network more quickly. The following conditions are possible: 0 LED off 1 LED on 2 blinks slowly 3 blinks rapidly
Firmware Version	State	The firmware version of the hardware module is shown in this server.
Firmware Status	State	In this server, the status bits of the FW are shown. The respective bits mean the following: Bit 1 DC not OK Bit 2 no Sync available Bit 3 Flash Data CRC Error Bit 4 Ram Data CRC Error Bit 5 invalid EEProm version Bit 6 Bus cycle time not supported Bit 7 Toggle Bit. Changes when new data is read from the module or before data is written to the module. Bit 8 not used Bit 9 not used Bit 10 data are valid
Required	Property	This client is active by default, which means that the S-DIAS hardware module at this position is mandatory for the system and can under no circumstances be disconnected or return an error. Otherwise, the entire hardware deactivates. If the hardware module is missing or removed, an S-DIAS error is triggered. If this client is initialized with 0, the hardware module located in this position is not mandatory. This means that it can be inserted or removed at any time. However, which components identified as "not required" should be selected with regard to the safety of the system.
Voltage 24 OK	State	Indicates whether the digital output supply voltage is OK 0 not OK 1 OK

Time Offset Error Bits	State	Bit 1 ... The time offset settings for the analog inputs were invalid and have been adjusted by the firmware automatically. This can happen when the distance between two time offsets is too short (less than 15 µs).

20.1.2 Digital Inputs and Outputs

Input [1-6]	Input	Shows the status of the digital input [1-6].
Input [7-14]	Input	Shows the back-read status of the digital outputs [1-8].
Output [1-8]	Output	With this server, the digital output [1-8] can be controlled. The output is set via the write method of the server.

20.1.3 Analog Inputs

AI1 Config Type	Property	0 AI1 used as analog input (Range: -10 V to +10 V). 1 AI1 used as analog input (Range: 0 V to +10 V) DEACTIVATED_LSL, 16#FFFF = input is disabled. As an initialization value
AI2 Config Type	Property	0 AI2 used as analog input (Range: 0 mA to 20 mA). 1 AI2 used as analog input (Range: 4 mA to 20 mA). DEACTIVATED_LSL, 16#FFFF = input is disabled. As an initialization value
AI[1-2] cut off frequency	Property	In this client, the cutoff frequency for the software low pass filter is set. Value setting options are: 0 Filter deactivated 1 10000 Hz 2 5000 Hz 3 1000 Hz 4 500 Hz 5 100 Hz 6 50 Hz 7 25 Hz 8 10 Hz 10-10000 10-10000 Hz sonst Filter deactivated As an initialization value

AI[1-2] minimum value	Property	This value indicates the minimum value for the channel. If the minimum value is measured at the channel (depending on AI[1-2] config), this value is output in the software. The range of the measurement values are defined by the setting in the clients AI[1-2]_Min + AI[1-2]_Max. As an initialization value
AI[1-2] maximum value	Property	This value indicates the maximum value for the channel. If the maximum value is measured at the channel (depending on AI[1-2] config), this value is output in the software. The range of the measurement values are defined by the setting in the clients AI[1-2]_Min + AI[1-2]_Max. As an initialization value
Analog Input [1-2]	Input	Analog input 1-2, status query over read().
AI2 low range limit	Property	Definable limit for detecting the lower measurement limit for AI2 (cable-break detection). Value range: 0-4000 [µA]. (3000 default value= 3 mA) As an initialization value

20.1.4 Communication Interfaces

ALARM	Downlink	With this downlink the corresponding alarm class can be placed via the hardware editor.

20.2 Time Trigger – Mode

In Time Trigger mode, the output value is set to a defined time point.
The configuration method must be called in during the Init for each digital output operated in the Time Trigger mode. The non-configured digital outputs can be operated via the server Output [1-8].
Methods per digital output:
Configuration methods: “DigitalOut_ConfigTimeTrigger”
Method for setting the time point: “DigitalOut_SetTimeTrigger”

In Time Trigger mode, the input value read at a defined time point.
The configuration method must be called in during the Init for each analog input operated in the Time Trigger mode. A combination of the Time Trigger mode and the AI[1-2] server is not possible.
Methods per analog input:
Configuration methods: „AnalogIn_ConfigTimeTrigger“
Method for setting the time point: „AnalogIn_SetTimeTrigger“
Method for reading the values: „AnalogIn_GetValues“

20.3 Latch - Modus

In Latch mode, a time stamp is set due to a latch event at the input.
The configuration method must be called in during the Init for each digital input operated in Latch mode. The non-configured digital inputs can be read via the server Input [1-14].
Digital input latch events: rising/falling edge.
Methods per digital input:
Configuration methods: “DigitalIn_ConfigLatch”
Method for reading the values: “DigitalIn_GetValues”

The configuration method must be called in during the Init for each analog input operated in the Latch mode. The non-configured analog inputs can be read via the server AI[1-14].
Latch events per analog input: rising/falling edge with adjustable voltage thresholds.
Methods per analog input:
Configuration methods: „AnalogIn_ConfigLatch“
Method for reading the values: „AnalogIn_GetValues“

Important

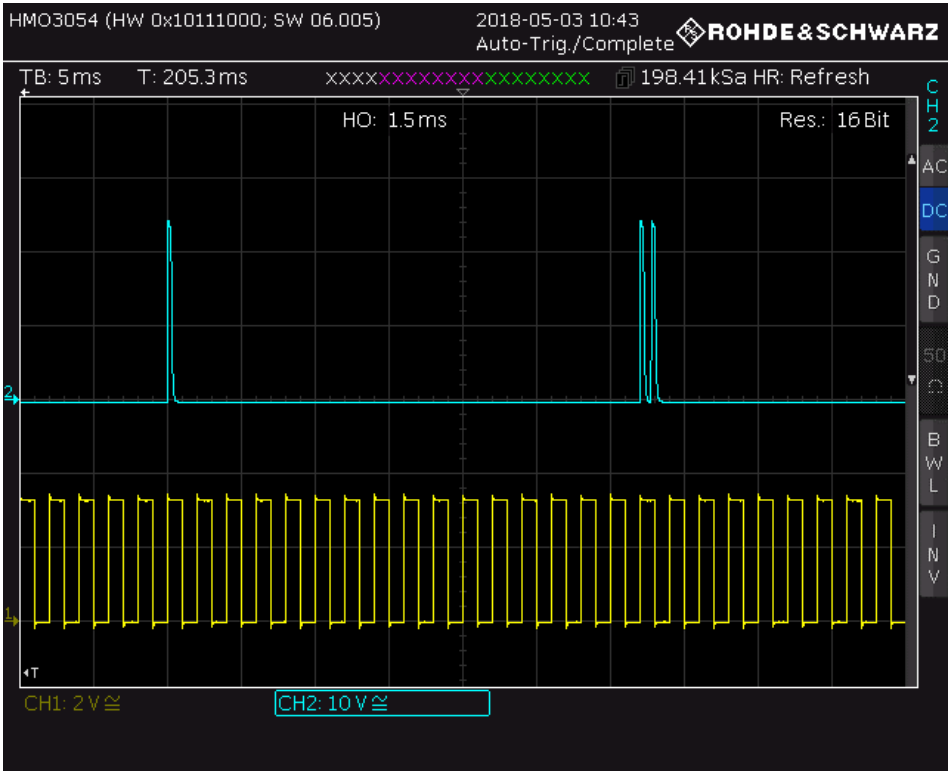
- A combination of the Time Trigger and Latch mode is not possible for the analog inputs.
- The configuration methods must be called during the Init.
- The methods for setting the time stamp and retrieving the values must be called from the realtime task.
- The IO011S module requires the SDIAS Manager protocol version 1.2.0. If this version is not installed, the module does not work and shows “_ClientNotready” or "_DOHandleInvalid" in the “ClassState” server. This version can be checked in the hardware class SdiasPLC, VI021, VI022 in the “ManagerProtocolVersion”. If no protocol version is shown in the server, the CPU operating system must be updated. If a protocol version lower than 1.2.0 is displayed, the FPGA and Firmware of the CPU or VI021, VI022 must be updated.
- The module only supports bus cycle times to a minimum of 0.5 ms! Operation with shorter times is not possible. In this case, "_ClientNotready" is shown in the “ClassState” server.

20.4 Hardware Time

All times stamps set and read are based on the hardware time stamp. This is returned by the “GetHWTimeStamp“ method (2-byte time, resolution µs). This is based on the start of each realtime cycle.

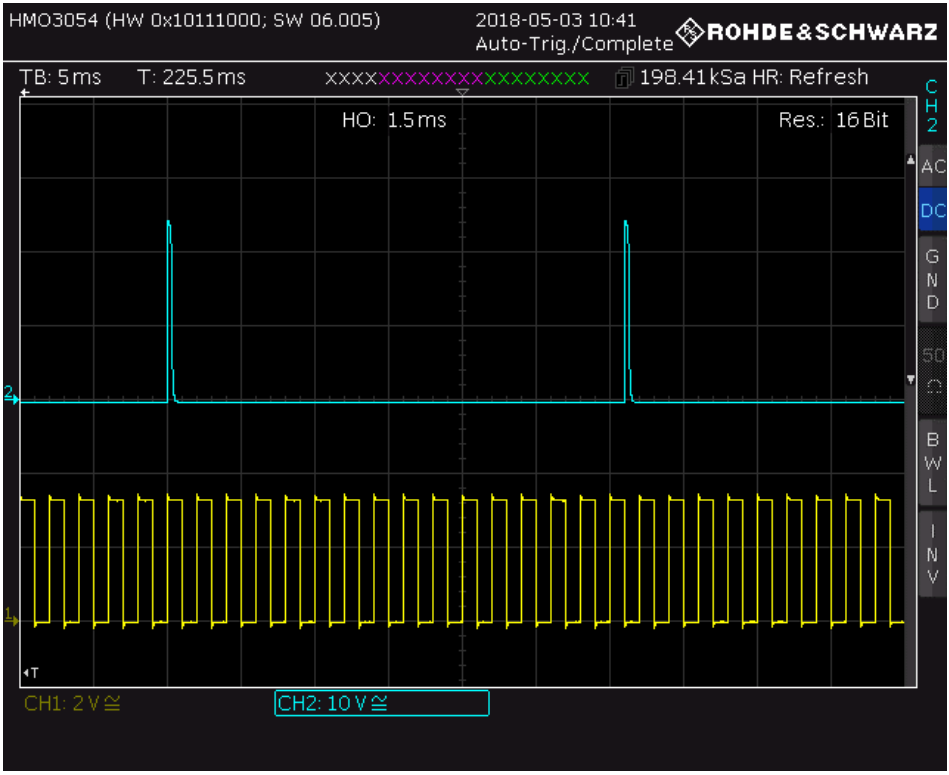
The time points set in Time Trigger mode must be greater than the hardware time stamp, since the transfer to the module occurs according to the realtime task.
The “GetTimeTriggerMinOffset” method returns the minimum time offset (resolution µs). This offset must be included, so that a time point can be correctly accepted by the module. This offset does not change during runtime and must be retrieved only once.
The time offset depends on the position of the module and can differ between modules. (e.g. module operated on local SDIA bus, module is operated behind a VI021.)
Time points set in the Time Trigger mode sent to the module in a 15-bit resolution! For this reason time points can only be set up to 32767 in the future. The hardware class calculates all time stamps measured to 16 bits = 2 bytes high.
The time stamps can be pre-calculated over several bus cycles. The “DigitalOut_SetTimeTrigger” and “AnalogIn_SetTimeTrigger” methods therefore do not have to be called every realtime cycle. After the last time stamp has been set to the module, the hardware class keeps the last output value sent. The command to hold the output is sent one bus cycle after the last time stamp is set. Only time stamps that are 32767 µs minus the bus cycle time in the future can be defined. If this condition is not met, a counter overflow can occur.

Example 1, error: A digital output with 4 registers is configured. The output is turned on/off at 0 ms and 32 ms. Since the counter overflows at 32.7 ms, an additional on/off process is run.



Blue: digital output
Yellow: 1ms Sync signal

Example 2, correct: A digital output with 4 registers is configured. The output is turned off at 0 ms and 31 ms. The output is stopped with the Sync at 32 ms. No additional switching processes are triggered.



Blue: digital output
Yellow: 1ms Sync signal

20.4.1 GetHWTimeStamp

Transfer parameters	Type	Description
none		
Return parameters	**Type**	**Description**
HWTimeStamp	UINT	Hardware time stamp in µs. This is based on the start of each realtime cycle. If the time stamp cannot be determined, the constant 0 is returned.

20.4.2 GetTimeTriggerMinOffset

Transfer parameters	Type	Description
none		
Return parameters	**Type**	**Description**
dMinOffset	DINT	-1 Offset could not be determined. >0 minimum time offset between the current hardware time stamp and the next switching time point for the module in µs.

20.5 Global Methods

The following method can be called via the ClassState server.

20.5.1 DigitalOut_ConfigTimeTrigger

Transfer parameters	Type	Description
OutputNr	DINT	Selects the digital output configured in the Time Trigger mode. Permissible values: 1-8
SampleNr	DINT	Configures the maximum possible number or switching process per bus cycle. Permissible values: 1-63
Return parameters	**Type**	**Description**
retval	DINT	0 Configuration successful. -1122 Input parameter “OutputNr” exceeds the allowed range. (1-8) -1123 Input parameter “SampleNr” exceeds the allowed range. (1-63) -1126 Method was called at the end of the Init.

NewInst call: _SMARTIO_DIGITALOUT_CONFIGTIMETRIGGER,
See SmartIO.h, Type: t_SmartIO_DigitalOut_ConfigTimeTrigger1

This method is used to configure a digital output in the Time Trigger mode.
If a digital output is configured in the Time Trigger mode, it can then only be activated via the “DigitalOut_SetTimeTrigger”. The write method of the corresponding output server “Output [1-8]” is deactivated in this case and in this server, the value 16#80000010 is displayed.
The maximum possible number of switching processes per bus cycle is limited to 64. These 64 available switching processes can be distributed over the individual outputs as desired.
Examples of digital output configurations:

output 1	output 2	output 3	output 4	output 5	output 6	output 7	output 8	Total	Allowed
8	8	8	8	8	8	8	8	64	Yes
2	2	2	2	2	2	2	2	16	Yes
16	16	16	16	0	0	0	0	64	Yes
0	32	0	0	0	32	0	0	64	Yes
63	0	1	0	0	0	0	0	64	Yes
16	16	16	16	16	16	16	16	128	No
63	0	0	0	0	63	0	0	126	No
0	0	0	0	64	0	0	0	64	No (only 63 per output!)

20.5.2 DigitalOut_SetTimeTrigger

Transfer parameters	Type	Description
OutputNr	DINT	Selects the digital output specified by the Time Trigger switching time point. Permissible values: 1-8
SampleNr	DINT	Number of switching time points sent. ≤0: Current status of the output is stopped (HIGH, LOW) until this method is recalled. 1-63: Number of switching time points sent. (The maximum number of switching time points is defined in the "DigitalOut_ConfigTimeTrigger" method.)
pValues	BOOL^	Pointer to the output values (HIGH/LOW). pValue^: 1st for output (TRUE / FALSE) (pValue + 1)^: 2nd for output (TRUE / FALSE) (pValue + 2)^: 3rd for output (TRUE / FALSE) … The number "SampleNr" must be sent to values.
pTimeTriggers	UINT^	Pointer to the switching time points pValue^: 1st switching time point for the output. [µs] (pValue + 2)^: 2nd switching time point for the output. [µs] (pValue + 4)^: 3rd switching time point for the output. [µs] … The number "SampleNr" must be sent to switching time point.
Return parameters	**Type**	**Description**
retval	DINT	0: Switching time point set successfully. -1020: The Pointer "pValues" or "pTimeTriggers" is invalid. -1022: Input parameter "OutputNr" exceeds the allowed range. (1-8) -1023: Input parameter "SampleNr" exceeds the allowed range. (1- value configured in "DigitalOut_ConfigTimeTrigger") -1026: Method called during the Init (The module is not yet configured)

NewInst call: _SMARTIO_DIGITALOUT_SETTIMETRIGGER,
See SmartIO.h, Type: t_SmartIO_DigitalOut_SetTimeTrigger1

With this method, the switching time points and the corresponding output values for the digital output are set. The switching time points must be sorted chronologically.
Switching time points can be set, which extend beyond a bus cycle.
For example, this method can only be called every 10 ms. The transferred timestamp can

thereby be 10 ms in the future. The timestamp can be a maximum of 32767 µs (15 bits) minus the bus cycle time in the future.

20.5.3 DigitalIn_ConfigLatch

Transfer parameters	Type	Description
InputNr	DINT	Selects the digital input configured in Latch mode. 1-6: Digital input 1-6 7-14: Back-reading of digital outputs 1.8
SampleNr	DINT	Configures the maximum possible number or Latch processes per bus cycle Permissible values: 1-63
EdgeTyp	DINT	Configures the edge at with to latch. 1: Rising edge 2: Falling edge 3: Rising and falling edge
Return parameters	**Type**	**Description**
retval	DINT	0: Configuration successful -822: Input parameter “InputNr” exceeds the allowed range. (1-14) -823: Input parameter “SampleNr” exceeds the allowed range. (1-63) -826: Method was called at the end of the Init -827: Input parameter “EdgeTyp” exceeds the allowed range. (1-3)

NewInst call: _SMARTIO_DIGITALIN_CONFIGLATCH,
See SmartIO.h, Type: t_SmartIO_DigitalIn_ConfigLatch1

This method is used to configure a digital input in latch mode.
The maximum possible number of Latch processes per bus cycle is limited to 128. These 128 available Latch processes can be distributed over the individual inputs as desired.
See example table for “DigitalOut_ConfigTimeTrigger” (instead of 64, a total of 128 latches are available for the inputs).

20.5.4 DigitalIn_GetValues

Transfer parameters	Type	Description
InputNr	DINT	Selects the digital input from which the value is back-read. 1-6: Digital input 1-6 7-14: Back-reading of digital outputs 1.8
SampleNr	DINT	Number of measurement values to return Permissible values: 1-63 .. (The maximum number of measurement values is defined in the “DigitalIn_ConfigLatch” method.)
SampleOffset	DINT	Offset of the measurement values to return. Using this parameter, measurement values can be skipped. The measurement values are returned starting from “SampleOffset”. Permissible values: 0-63 (The maximum number of measurement values is defined in the “DigitalIn_ConfigLatch” method.)
pDataTime	^UINT	Pointer to the measured time points The hardware class writes the measured time points to this address. A “SampleNr” * 2-byte memory space must be provided. If less the value of “SampleNr” edges were measured, the last measured time point in mirrored in the underlying memory space. The information as to whether a flank was detected is returned in “pDataEdge”. Return values: pDataTime^: Timestamp of the 1st edge (pDataTime 2)^: + Timestamp of the 2nd edge (pDataTime 4)^: + Timestamp of the 3rd edge …
pDataEdge	^BSINT	Pointer to the measured edges. The hardware class writes the measured edge information to this address. A “SampleNr” * 1-byte memory space must be provided. Possible return values per measurement value: 0: No edge (less than the value of “SampleNr” was measured) 1: Rising edge 2: Falling edge Return values: pDataEdge^: Edge information of the 1st edge (pDataEdge 1)^: + Edge information of the 2nd edge (pDataEdge 2)^: + Edge information of the 3rd edge ...
Return parameters	**Type**	**Description**

retval	DINT	0 Measurement values are valid. -920 One of the input parameters “pDataTime”, “pDataEdge” is NIL -921 The input was not configured in Latch mode. (See: “DigitalIn_ConfigLatch”) -922 Input parameter “InputNr” exceeds the allowed range. (1-14) -923 Input parameter “SampleNr” exceeds the allowed range. (1-63) -926 Method called during the Init (The module is not yet configured)

NewInst call: _SMARTIO_DIGITALIN_GETVALUES,
See SmartIO.h, Type: t_SmartIO_DigitalIn_GetValues1

This method returns the time point as well as the edge information of a digital input.

20.5.5 AnalogIn_ConfigTimeTrigger

Transfer parameters	Type	Description
InputNr	DINT	Selects the analog input configured in the Time Trigger mode. Permissible values: 1-2
SampleNr	DINT	Configures the maximum possible number or measurement values per bus cycle Permissible values: 1-8
Return parameters	**Type**	**Description**
retval	DINT	0 Configuration successful -221 The memory for the configuration of analog inputs could not be allocated -222 Input parameter “InputNr” exceeds the allowed range. (1-2) -223 Input parameter “SampleNr” exceeds the allowed range. (1-8) -224 The analog inputs are already configured in latch mode. A combination of the Time Trigger and Latch mode is not possible for the analog inputs -226 Method was called at the end of the Init

NewInst call: _SMARTIO_ANALOGIN_CONFIGTIMETRIGGER,
See SmartIO.h, Type: t_SmartIO_Analogin_ConfigTimeTrigger1

This method is used to configure an analog input in Time Trigger mode.
The maximum possible number of measurements is limited to 8. These 8 available measurements can be distributed over the individual inputs as desired.

Example configuration of the analog inputs:

input 1	input 2	Total	Allowed
8	0	8	Yes
6	2	8	Yes
4	4	8	Yes
0	4	4	Yes
2	0	2	Yes
8	8	16	No

20.5.6 AnalogIn_ConfigLatch

Transfer parameters	Type	Description
InputNr	DINT	Selects the analog input configured in Latch mode. Permissible values: 1-2
SampleNr	DINT	Configures the maximum possible number or measurement values per bus cycle Permissible values: 1-8
pEdgeTyp	^BSINT	Configures the edges at which to latch. Permissible values per measurement value: 1 Rising edge 2 Falling edge 3 Rising and Falling edge Pointer to the configuration: pValue^ Edge configuration for the 1st measurement (pValue + 1)^ Edge configuration for the 2nd measurement (pValue + 2)^ Edge configuration for the 3rd measurement … The number “SampleNr” must be sent to values.
pLowerThreshold	^DINT	Configures the lower limit at which to latch. The specified analog limits are converted via the analog input configuration. See: AI[1-2] Config Type, AI[1-2] minimal value, AI[1-2] maximal value. Pointer to the configuration: pValue^ Lower limit for the 1st measurement (pValue + 4)^ Lower limit for the 2nd measurement (pValue + 8)^ Lower limit for the 3rd measurement … The number “SampleNr” must be sent to values.

pUpperThreshold	^DINT	Configures the upper limit at which to latch. The specified analog limits are converted via the analog input configuration. See: AI[1-2] Config Type, AI[1-2] minimal value, AI[1-2] maximal value. Pointer to the configuration: pValue^ — Upper limit for the 1st measurement (pValue + 4)^ — Upper limit for the 2nd measurement (pValue + 8)^ — Upper limit for the 3rd measurement … The number “SampleNr” must be sent to values.
Return parameters	**Type**	**Description**
retval	DINT	0 — Configuration successful -320 — One of the input parameters “pEdgeTyp”, “pLowerThreshold”, “pUpperThreshold” is NIL -321 — The memory for the configuration of analog inputs could not be allocated -322 — Input parameter “InputNr” exceeds the allowed range. (1-2) -323 — Input parameter “SampleNr” exceeds the allowed range. (1-8) -324 — The analog inputs are already configured in Time Trigger mode. A combination of the Time Trigger and Latch mode is not possible for the analog inputs. -325 — The scaling factors for the analog inputs are selected incorrectly. (AI[1-2] minimal value = AI[1-2] maximal value) -326 — Method was called at the end of the Init

NewInst call: _SMARTIO_ANALOGIN_CONFIGLATCH,
See SmartIO.h, Type: t_SmartIO_Analogin_ConfigLatch1

This method is used to configure an analog input in Latch mode.
The maximum possible number of measurements is limited to 8. These 8 available measurements can be distributed over the individual inputs as desired.
See example table for “AnalogIn_ConfigTimeTrigger”.

20.5.7 AnalogIn_SetTimeTrigger

Transfer parameters	Type	Description
InputNr	DINT	Selects the analog input specified in the Time Trigger measurement time point. Permissible values: 1-2
SampleNr	DINT	Number of measurement time points sent. 1-8: Number of measurement time points sent. (The maximum number of measurement time points is defined in the “AnalogIn_ConfigLatch” method)
pTimeTriggers	UINT^	Pointer to the measurement time points pValue^: 1st measurement time point for the input. [µs] (pValue + 2)^: 2nd measurement time point for the input. [µs] (pValue + 4)^: 3rd measurement time point for the input. [µs] … The number “SampleNr” must be sent to switching time point.
Return parameters	**Type**	**Description**
retval	DINT	0: Switching time point set successfully -120: The specified pointer “pTimeTriggers” is invalid -122: Input parameter “InputNr” exceeds the allowed range. (1-2) -123: Input parameter “SampleNr” exceeds the allowed range. (1- value configured in “AnalogIn_ConfigTimeTrigger”) -124: The analog input is not in Time-Trigger mode (“AnalogIn_ConfigTimeTrigger” was not called) -126: Method called during the Init (The module is not yet configured)

NewInst call: _SMARTIO_ANALOGIN_SETTIMETRIGGER,
See SmartIO.h, Type: t_SmartIO_Analogin_SetTimeTrigger1

With this method, the measurement time points for an analog input are set.
Switching time points can be set, which extend beyond a bus cycle.
For example, this method can only be called every 10 ms. The transferred timestamp can thereby be 10 ms in the future. The timestamp can be a maximum of 32767 µs (15 bits) minus the bus cycle time in the future.

20.5.8 AnalogIn_GetValues

Transfer parameters	Type	Description
InputNr	DINT	Selects the analog input from which the values are back-read. Permissible values: 1-2
SampleNr	DINT	Number of measurement values to return. 1-8 The maximum number of measurement values is defined in the “AnalogIn_ConfigLatch” or “AnalogIn_ConfigTimeTrigger” method.
SampleOffset	DINT	Offset of the measurement values to return. Using this parameter, measurement values can be skipped. The measurement values are returned starting from “SampleOffset”. 0-8 The maximum number of measurement values is defined in the “AnalogIn_ConfigLatch” or “AnalogIn_ConfigTimeTrigger” method.
pDataValue	^DINT	Pointer to the measured analog values. Input parameter is used in Time Trigger mode only. The hardware class writes the measured analog values to this address. A “SampleNr” * 4-byte memory space must be provided. The returned analog values are converted via the analog input configuration. See: AI[1-2] Config Type, AI[1-2] minimal value, AI[1-2] maximal value. If no analog value was latched, the value 16#80000010 is returned. Return values: pDataValue^ Value of the 1st measurement (pDataValue + 4)^ Value of the 2nd measurement (pDataValue + 8)^ Value of the 3rd measurement ...
pDataTime	^UINT	Pointer to the measured time points The input parameter is used in Latch mode only. The hardware class writes the measured time points to this address. A “SampleNr” * 2-byte memory space must be provided. The information as to whether a flank was detected is returned in “pDataEdge”. Return values: pDataTime^ Timestamp of the 1st measurement (pDataTime + 2)^ Timestamp of the 2nd measurement (pDataTime + 4)^ Timestamp of the 3rd measurement …

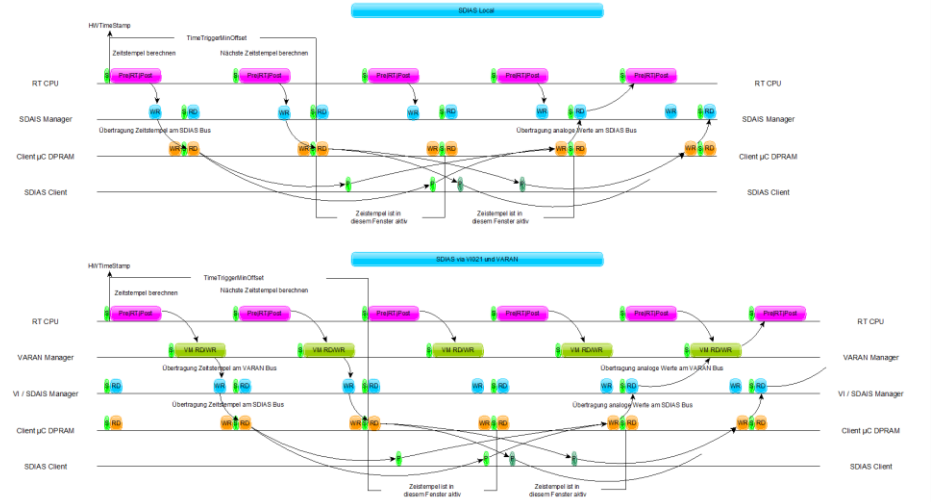
<table>
<tr><td>pDataEdge</td><td>^BSINT</td><td>Pointer to the measured edges. The input parameter is used in Latch mode only. The hardware class writes the measured edge information to this address. A “SampleNr” * 1-byte memory space must be provided.
Possible return values per measurement value:<table><tr><td>0</td><td>No edge (no edge was measured for this measuring point).</td></tr><tr><td>1</td><td>Rising edge</td></tr><tr><td>2</td><td>Falling edge</td></tr></table>Return values:<table><tr><td>pDataEdge^</td><td>Edge information of the 1st measurement</td></tr><tr><td>(pDataEdge + 1)^</td><td>Edge information of the 2nd measurement</td></tr><tr><td>(pDataEdge + 2)^</td><td>Edge information of the 3rd measurement</td></tr><tr><td>...</td><td></td></tr></table></td></tr>
<tr><th>Return parameters</th><th>Type</th><th>Description</th></tr>
<tr><td>retval</td><td>DINT</td><td><table><tr><td>0</td><td>Measurement values are valid</td></tr><tr><td>-420</td><td>One of the input parameters “pDataTime”, “pDataEdge” is NIL and the input is in Latch mode</td></tr><tr><td>-420</td><td>The input parameter “pDataValue” is NIL and the input is in Time Trigger Modus</td></tr><tr><td>-421</td><td>The input was not configured. (See “AnalogIn_ConfigLatch” or „AnalogIn_ConfigTimeTrigger“)</td></tr><tr><td>-422</td><td>Input parameter “InputNr” exceeds the allowed range. (1-14)</td></tr><tr><td>-423</td><td>Input parameter “SampleNr” exceeds the allowed range. (1-8)</td></tr><tr><td>-424</td><td>No input was configured. (See “AnalogIn_ConfigLatch” or “AnalogIn_ConfigTimeTrigger”)</td></tr><tr><td>-426</td><td>Method called during the Init (The module is not yet configured)</td></tr></table></td></tr>
</table>

NewInst call: _SMARTIO_ANALOGIN_GETVALUES,
See SmartIO.h, Type: t_SmartIO_Analogin_GetValues1

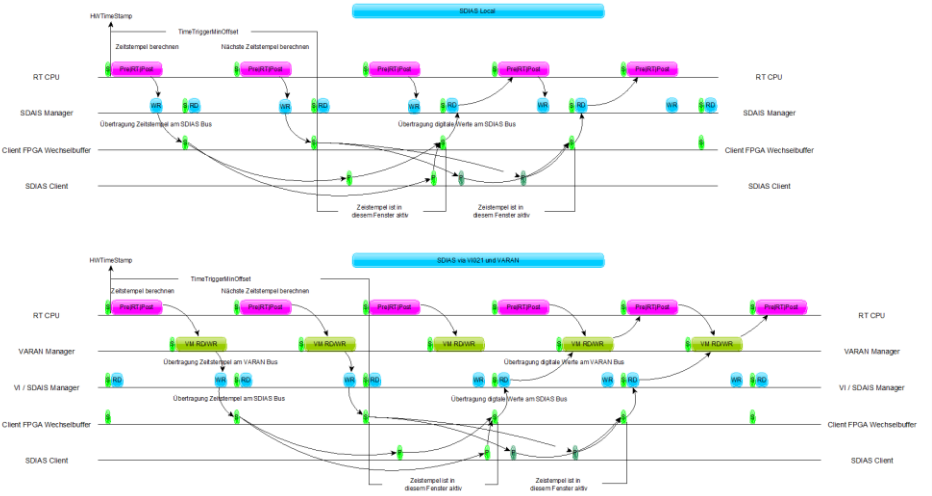
This method returns the time point, as well as the edge information of an analog input if it is in Latch mode.
This method returns the analog values of an analog input if it is in Time Trigger mode.

20.6 Time Response

20.6.1 Analog Values



20.6.2 Digital Values



Documentation Changes

Change date	Affected page(s)	Chapter	Note
09.07.2019	10	1.9 S-DIAS Protocol Version	Chapter added
21.10.2019	10	1.9 S-DIAS Protocol Version	Note about operating system version added
14.11.2019	38	11 Supported Cycle Times	Chapter added
28.02.2020	38	11 Supported Cycle Times	Text adapted
08.09.2020	40	12 Hardware Class IO011S	Chapter added
04.11.2020	22	5 Mounting	Expansion functional ground connection
06.12.2022	12	1.7 Miscellaneous	UKCA conformity
26.07.2023		Document	General chapters added, design