VARAN Client Board VEB 011C

Versatile **A**utomation **R**andom **A**ccess **N**etwork

This Client Board serves to easily equip all kinds of periphery devices with the VARAN bus. Data exchange can be done via CANopen or DPRAM.

Technical Data

Performance Data

Internal memory	Serial 4-MBit-Flash
Interfacing	1 x VARAN (Client) (maximum length: 100 m) 1 x Periphery interface
Connection to periphery module	Over 50-pin. Board-to-Board-connector plug, 0.8 mm spacing (Type ERNI Microstac, order no.: 114713)

Electrical Requirements

Internal supply voltage (VDD)	Typically +3.3 V DC (±4 %) (Supplied by the periphery module over the 50-pin connector plug)
Current consumption of the voltage supply	Minimum 250 mA (Depending on the external circuit)

Miscellaneous

Article number	16-081-011C
Hardware version	1.x

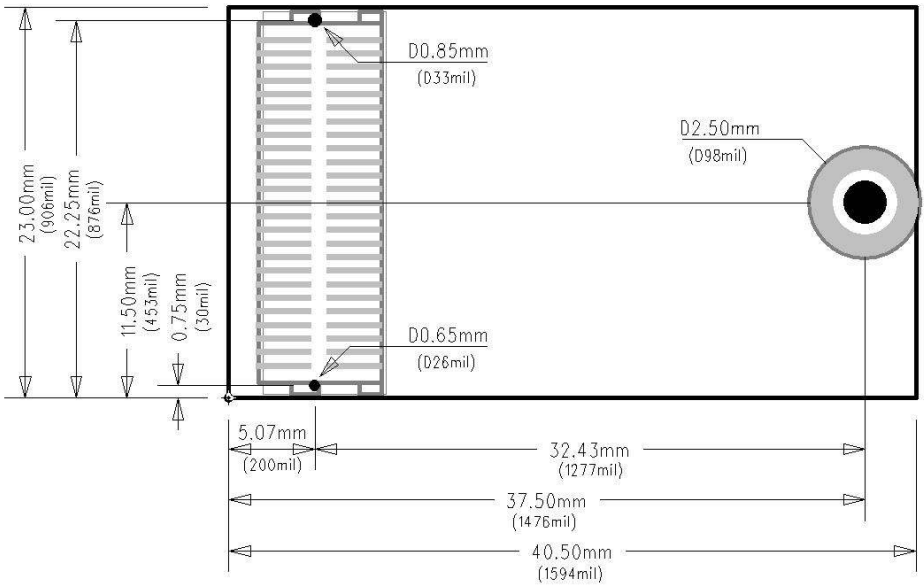
Environmental Conditions

Storage temperature	-20 – +85 °C
Operating temperature [1)]	0 – 85 °C
Humidity	0 – 95 %, uncondensed
EMV stability	[2)]
Shock resistance	150 m/s²

[1)] According to component specifications. The operating temperature of the complete device has to be specially defined for each application since the operating temperatures (mounting position, housing, heat sources near the VEB) are not known.

[2)] The EMV stability has to be tested separately in the complete system for each application.

Mechanical Dimensions



The dimensioning of the center holes of the 50-pole ERNI Board-to-Board connector is effective for the plugs on the base board (doesn't show the position of the connectors on the VEB).

The VEB is shown from the connector back side in this illustration.

The height of the component parts on the base board under the VEB must not exceed 3 mm.

1 Basics

There are several modes to choose from as can be seen in 0. The mode can be adjusted with 3 pins by hardware (see pin assignment 2.1) and can also be overwritten by software (see address mapping 2.2.1).

This document is designed to support the programmer. All relevant information to implement a client/program should be contained.

1.1 Connector

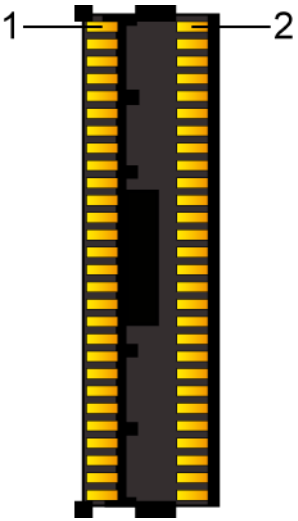


Figure 3: Connector

2 Programming Guidelines

2.1 VEB011C Pins

Pin	Identifier	DPRAM Mode		DPRAM Mode auto-increment		CANopenMode		CANopenMode auto-increment	
1		GND		GND		GND		GND	
2		GND		GND		GND		GND	
3	V2	D0	IO	D0	IO	D0	IO	D0	IO
4	V1	-		-		-		-	
5	V4	D1	IO	D1	IO	D1	IO	D1	IO
6	V3	-		-		-		-	
7	V6	D2	IO	D2	IO	D2	IO	D2	IO
8	V5	-		-		-		-	
9	V8	D3	IO	D3	IO	D3	IO	D3	IO
10	V7	-		-		-		-	
11	V10	D4	IO	D4	IO	D4	IO	D4	IO
12	V9	IRQ	Out	IRQ	Out	IRQ	Out	IRQ	Out
13	V12	D5	IO	D5	IO	D5	IO	D5	IO
14	V11	Mode0		Mode0		Mode0		Mode0	
15	V14	D6	IO	D6	IO	D6	IO	D6	IO
16	V13	Mode1		Mode1		Mode1		Mode1	
17	V16	D7	IO	D7	IO	D7	IO	D7	IO
18	V15	Mode2		Mode2		Mode2		Mode2	
19		VDD		VDD		VDD		VDD	
20		VDD		VDD		VDD		VDD	
21		GND		GND		GND		GND	
22	V17	Ready	Out	Ready	Out	Ready	Out	Ready	Out
23		Phy_RX+		Phy_RX+		Phy_RX+		Phy_RX+	
24	V18	Sync	Out	Sync	Out	Sync	Out	Sync	Out
25		Phy_RX-		Phy_RX-		Phy_RX-		Phy_RX-	
26	V19	A0	In	A0	In	A0	In	A0	In
27		Phy_TX+		Phy_TX+		Phy_TX+		Phy_TX+	
28	V20	A1	In	A1	In	A1	In	A1	In
29		Phy_TX-		Phy_TX-		Phy_TX-		Phy_TX-	
30	V21	A2	In	-		A2	In	-	
31		VB +3V3		VB +3V3		VB +3V3		VB +3V3	
32	V22	A3	In	-		A3	In	-	
33	V24	CLK 25 MHz	Out	CLK 25 MHz	Out	CLK 25 MHz	Out	CLK 25 MHz	Out
34	V23	A4	In	-		A4	In	-	
35	V26	/Periphery Reset	Out	/Periphery Reset	Out	/Periphery Reset	Out	/Periphery Reset	Out
36	V25	A5	In	-		A5	In	-	
37	V28	-		-		-		-	
38	V27	A6	In	--		A6	In	-	
39	V30	R / W	In	R / W	In	R / W	In	R / W	In

40	V29	A7	In	--		A7	In	-	
41	V32	-		-		-		-	
42	V31	A8	In	--		A8	In	-	
43		/Phy_led_link		/Phy_led_link		/Phy_led_link		/Phy_led_link	
44	V33	A9	In	--		A9	In	-	
45		/Phy_led_active		/Phy_led_active		/Phy_led_active		/Phy_led_active	
46	V34	A10	In	--		A10	In	-	
47	V36	-		-		-		-	
48	V35	A11	In	-		A11	In	-	
49		GND		GND		GND		GND	
50	V37	/CS	In	/CS	In	/CS	In	/CS	In

Table 1: Pins

2.1.1 Timing synchronous Manager to Client (MnPDO)

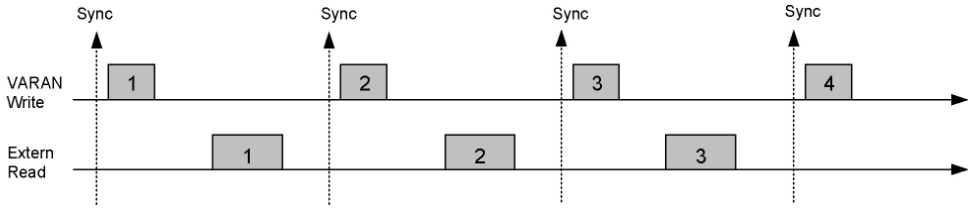


Figure 5: Client reads data from manager, synchronous

In this case the µC (Client) is synchronous to the VARAN system. It is the simplest case. Now the timings for faster and slower CPU's are considered.

2.1.2 Timing asynchronous (µC faster) Manager to Client (MnPDO)

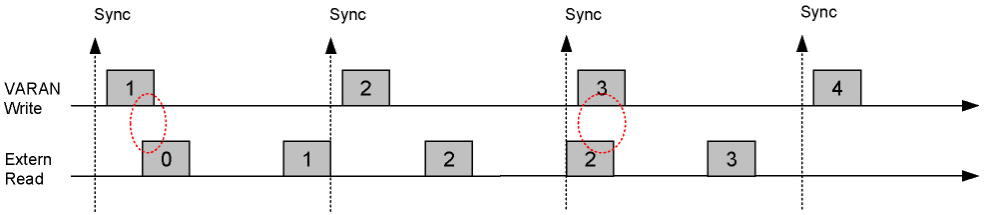


Figure 6: Client reads data from manager, asynchronous faster

In this case the µC (Client) works faster than the VARAN system. The interferences (marked) are the important events. As long as the new data are not written completely by the VARAN manager the old data are read by the client (possible because of the alternating buffer). This mechanism assures consistent data inventory.

2.1.3 Timing asynchronous (µC slower) Manager to Client (MnPDO)

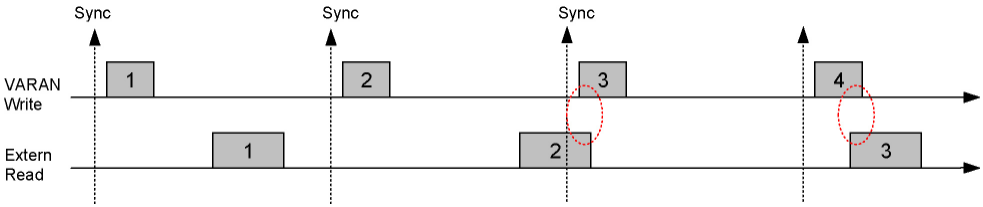


Figure 7: Client reads data from manager, asynchronous slower

In this case the µC (Client) works slower than the VARAN system. Consistent data inventory is achieved like in (2.1.2) above.

2.1.4 Critical Timing Manager to Client (MnPDO)

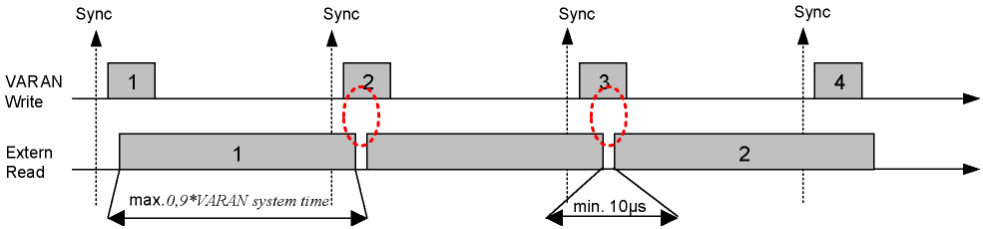


Figure 8: Critical Timing, client reads data from manager

The extern µC (Client) maximal read time is *0,9*VARAN system time* and the minimal delay between two procedures (write accesses) is *10µs*. Setting Bit 0 of the Switch Alternate Byte is a write access.

2.1.5 Timing synchronous Client to Manager (ClPDO)

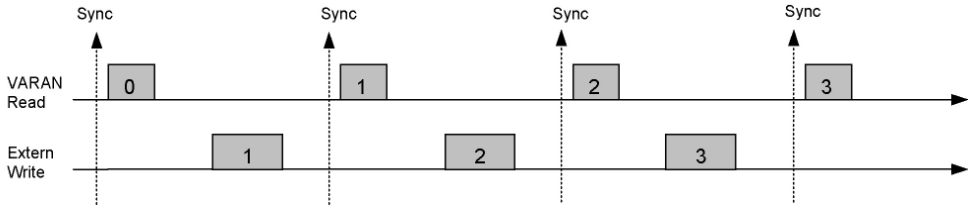


Figure 10: Client to Manager, synchronous

The µC (Client) is synchronous to the VARAN manager. Data written by the client in one period are read by the manager in the next period.

2.1.6 Timing asynchronous (µC faster) Client to Manager (ClPDO)

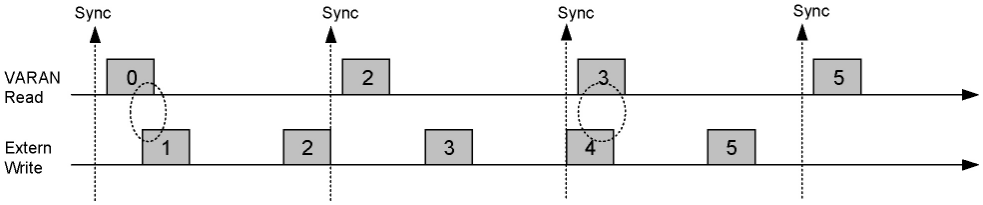


Figure 11: Client to Manager, asynchronous faster

In this case the µC (Client) is faster than the manager. The alternating buffer assures consistent data inventory. New data are only read by the manager if they are completely written by the client. As demonstrated with data package 4 it can happen that data sent by the client get overwritten before read by the manager.

2.1.7 Timing asynchronous (µC slower) Client to Manager (ClPDO)

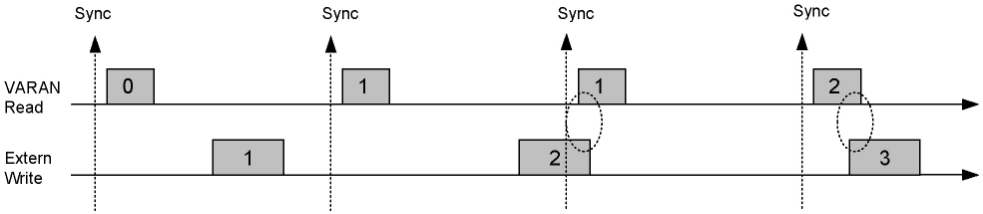


Figure 12: Client to manager, asynchronous slower

The µC (Client) is slower than the manager. Values are only read by the manager after a complete write access. This ensures consistent data inventory.

2.1.8 Critical Timing Client to Manager (ClPDO)

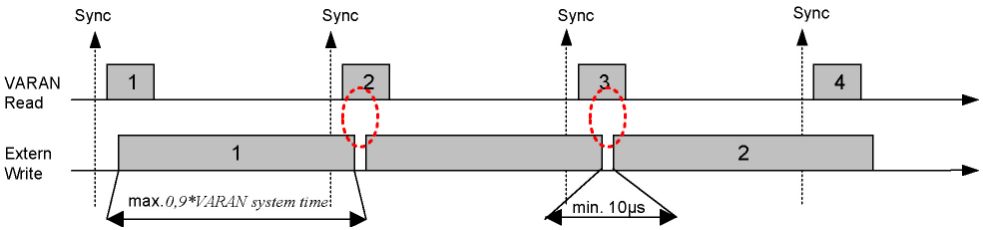


Figure 13: Critical Timing, Client to Manager

The maximum µC (Client) write time is *0,9*VARAN system time* and the minimal delay between the write accesses is *10µs*.

2.2 Address Mapping

2.2.1 CANopen Manager (not necessary for client side)

Address (hex)	Size (Byte)	Access Type:	Description	Reset value
Memory				
0000	2	r	Protocol Mode Bit 0: 1=CANopen, 0=Invalid Bit 1 to 15: Reserved	0001
0002	2	r	Start Address of VARAN Client Control Address Space	0800
0004	2	r	Start Address of MnPDO	0100
0006	2	r	Start Address of ClPDO	0180
0008	2	r	Start Address of MnSDO	0200
000A	2	r	Start Address of ClSDO	0280
000C	244	-	Reserved	
0100	16	-	MnPDO Reserved	
0110	1	r/w	MnPDO (Process Data Object Master to Client) Bit 0 to 5 : Message Counter Bit 6 to 7 : Reserved	
0111	1	r/w	MnPDO reserved for NMT	
0112	1	r/w	MnPDO Mapping	
0113	1	r/w	ClPDO Mapping	
0114	64	r/w	MnPDO Data	
0154	44	-	Reserved	
0180	16	-	ClPDO Reserved	
0190	1	r	ClPDO (Process Data Object Client to Master) Bit 0 to 5 : Message Counter Bit 6 : Reserved Bit 7 : Error	00
0191	1	r	ClPDO Nodestate	00
0192	1	r	MnPDO Mapping	00
0193	1	r	ClPDO Mapping	00
0194	64	r	ClPDO Data	00
01D4	44	-	Reserved	
0200	16	-	MnSDO Reserved	
0210	1	r/w	MnSDO (Service Data Object Master to Client) Bit 0 to 5 : Message Counter Bit 6 to 7 : Reserved	00
0211	1	r/w	MnSDO reserved for NMT	00

0212	64	r/w	MnSDO Data	00
0252	46	-	Reserved	
0280	16	-	ClSDO Reserved	
0290	1	r	ClSDO (Service Data Object Client to Master) Bit 0 to 5 : Message Counter Bit 6 : Reserved Bit 7 : Error	00
0291	1	r	ClSDO Nodestate	00
0292	64	r	ClSDO Data	00
02D2	1326	r/w	Reserved	
0800	2048	-	Reserved	
1000	2032	r/w	DPRAM	
17F0	2064	-	Reserved	
2000	1	r/w	VEB011 Mode Register Bit 7 .. 3 : Reserved Bit 2 .. 0 : Mode 000 Bus mode **(not available in VEB011C)** 001 IO mode **(not available in VEB011C)** 010 DPRAM mode without auto increment 011 DPRAM mode with auto increment 100 CANopen without auto increment 101 CANopen with auto increment	Mode pins
2001	1	r/w	Sync Mode Register Bit 7 .. 3 : Reserved Bit 2 : 1 = Enable tristate buffer for sync/veb_irq output Bit 1 : 1 = Sync/veb_irq output is active low, 0 = active high Bit 0 : 1 = Enable Sync Quitting Mode 0 = Enable Pulse width Register	00
2002	2	r/w	Sync Pulse width Register Bit 15 .. 0 : Value in steps of 20ns (e.g. 5 = 100ns)	0000

Table 2: Address Mapping Manager

2.2.2 CANopen mode (µC side)

Address (hex)	Size (Byte)	Access Type:	Description	Reset value
0000	2	r	Protocol Mode Bit 0: 1=CANopen, 0=Invalid Bit 1 to 15: Reserved	0001
0002	2	r	Start Address of VARAN Client Control Address Space	0800
0004	2	r	Start Address of MnPDO	0100
0006	2	r	Start Address of ClPDO	0180
0008	2	r	Start Address of MnSDO	0200
000A	2	r	Start Address of ClSDO	0280
000C	244	-	Reserved	
0100	16	-	MnPDO Reserved	
0110	1	r	MnPDO (Process Data Object Master to Client) Bit 0 to 5 : Message Counter Bit 6 to 7 : Reserved For handling the alternating buffer, read this register before NMT and data	00
0111	1	r	MnPDO reserved for NMT	00
0112	1	r	MnPDO Mapping	00
0113	1	r	ClPDO Mapping	00
0114	64	r	MnPDO Data	00
0154	44	-	Reserved	
0180	16	-	ClPDO Reserved	
0190	1	r/w	ClPDO (Process Data Object Client to Master) Bit 0 to 5 : Message Counter Bit 6 : Reserved Bit 7 : Error For handling the alternating buffer, write this register after nodestate and data	00
0191	1	r/w	ClPDO Nodestate	00
0192	1	r/w	MnPDO Mapping	00
0193	1	r/w	ClPDO Mapping	00
0194	64	r/w	ClPDO Data	00
01D4	44	-	Reserved	
0200	16	-	MnSDO Reserved	

0210	1	r	MnSDO (Service Data Object Master to Client) Bit 0 to 5 : Message Counter Bit 6 to 7 : Reserved Reading this register cleans DDOIRQ	00
0211	1	r	MnSDO reserved for NMT	00
0212	64	r	MnSDO Data	00
0252	46	-	Reserved	
0280	16	-	ClSDO Reserved	
0290	1	r/w	ClSDO (Service Data Object Client to Master) Bit 0 to 5 : Message Counter Bit 6 : Reserved Bit 7 : Error	00
0291	1	r/w	ClSDO Nodestate	00
0292	64	r/w	ClSDO Data	00
02D2	1326	r/w	Reserved	
0800	1792	r/w	VARAN Control Address Space See in VARAN Design Spec	
0F00	4	w32	Transmit FIFO Data Input	-
0F04	4	w32	Transmit FIFO Frame Length Write frame length before filling the FIFO Bit 10 .. 0 : Frame Length (in Bytes max. 1518)	-
0F08	4	r32	Receive FIFO Data Output	-
0F0C	4	r32	Receive FIFO Frame Length (in Bytes) 0 = no valid frame in FIFO	00000000
0F10	4	r	Available Registers in Transmit FIFO (in Bytes)	00000000
0F14	4	w	FIFO Control register Bit 0 : 1 = Reset Transmit FIFO Bit 1 : 1 = Reset Receive FIFO	-
0F14	4	r	FIFO Status register (IRQ Quit register) Bit 0 : 1 = frame transmitted Bit 1 : 1 = frame received (valid frame is in FIFO) Bit 2 : 1 = transmit FIFO error (Transmit FIFO Frame Length > 1518, or writing false values of bytes in FIFO) Bit 3 : 1 = receive FIFO error (Read Receive FIFO when no valid frame)	00000000
0F18	4	r/w	Interrupt enable register Bit 0 : 1 = frame transmitted Bit 1 : 1 = frame received Bit 2 : 1 = transmit FIFO error Bit 3 : 1 = receive FIFO error	00000000

0F1C	4	r/w	Receive MAC Filter register Bit 0 : 1 = Unicast enable (Destination address = MAC address) Bit 1 : 1 = Broadcast enable (Destination address = 16#FFFFFFFFFFFF) Bit 2 : 1 = Promiscuous enable (all destination address are received)	00000000
0F20	6	r/w	MAC Address	00000000 0000
0F26	1	r/w	Port Control / Link Status register Bit 0 : 1 = Link established (read only) Transmitting is only allowed, when Link is established Bit 1 : 1 = Port enable (Port must be enabled before transmitting)	00
0F27	187	-	Reserved	
0FE1	1	r/w	System IRQ Register Bit 0 : 1 = CANopen SDO data/message counter change Interrupt Bit 1 : 1 = EMAC Interrupt Bit 2 to 7 : Reserved	00
0FE2	1	-	Reserved	00
0FE3	1	r/w	System Interrupt Enable Register Bit 0 : 1 = CANopen SDO Interrupt enabled Bit 1 : 1 = EMAC Interrupt enabled	00
0FE4	12	-	Reserved	00
0FF0	1	w	Sync Quitting Register Bit 0 : 1 = Clears Sync interrupt Bit 1 to 7 : Reserved	00
0FF1	15	-	Reserved	

Table 3: Address Mapping Client

2.2.3 DPRAM Mode (µC side)

Address (hex)	*Size (Byte)*	*Access Type:*	*Description*	*Reset value*
0000	2048	r/w	DPRAM (In DPAM Mode)	00
0800	1792	r/w	VARAN Control Address Space See in VARAN Design Spec	
0F00	4	w32	Transmit FIFO Data Input	-
0F04	4	w32	Transmit FIFO Frame Length Write frame length before filling the FIFO Bit 10 .. 0 : Frame Length (in Bytes max. 1518)	-
0F08	4	r32	Receive FIFO Data Output	-

0F0C	4	r32	Receive FIFO Frame Length (in Bytes) 0 = no valid frame in FIFO	00000000
0F10	4	r	Available Registers in Transmit FIFO (in Bytes)	00000000
0F14	4	w	FIFO Control register Bit 0 : 1 = Reset Transmit FIFO Bit 1 : 1 = Reset Receive FIFO	-
0F14	4	r	FIFO Status register (IRQ Quit register) Bit 0 : 1 = frame transmitted Bit 1 : 1 = frame received (valid frame is in FIFO) Bit 2 : 1 = transmit FIFO error (Transmit FIFO Frame Length > 1518, or writing false values of bytes in FIFO) Bit 3 : 1 = receive FIFO error (Read Receive FIFO when no valid frame)	00000000
0F18	4	r/w	Interrupt enable register Bit 0 : 1 = frame transmitted Bit 1 : 1 = frame received Bit 2 : 1 = transmit FIFO error Bit 3 : 1 = receive FIFO error	00000000
0F1C	4	r/w	Receive MAC Filter register Bit 0 : 1 = Unicast enable (Destination address = MAC address) Bit 1 : 1 = Broadcast enable (Destination address = 16#FFFFFFFFFFFF) Bit 2 : 1 = Promiscuous enable (all destination address are received)	00000000

3 Mode Description

There are several modes to choose from. The following table specifies them. Also see the manager address mapping (2.2.1) and the pin assignment (2.1).

Mode2	*Mode1*	*Mode0*	*Mode*
0	0	0	"000" Bus Mode **(not available for VEB011C)**
0	0	1	"001" IO Mode **(not available for VEB011C)**
0	1	0	"010" DPRAM Mode (without address auto-increment)
0	1	1	"011" DPRAM Mode (with address auto-increment)
1	0	0	"100" CANopen Mode (without address auto-increment)
1	0	1	"101" CANopen Mode (with address auto-increment)

Table 4: Modes

3.1 DPRAM Mode

An external µC can access to the DPRAM, the Ethernet MAC or to the VARAN Control address space in the FPGA.

Also see 2.2.3

3.2 CANopen Mode

An external µC can access to the CANopen alternating buffer, the Ethernet MAC or to the VARAN Control address space in the FPGA.

Also see 2.2.2

3.3 Non auto-increment mode

In DPRAM and CANopen mode the usage of the pins the same. The bus supplies 12 bit address width and 8 bit data width. The combined Read/Write signal is read high active and write low active. The Chip select is low active. The Sync and Ready are high active.

3.4 Auto-increment mode

In DPRAM and CANopen mode the usage of the pins the same. The different to the non auto-increment mode is that only two address lines are used. This fact offers the possibility to save input/output ports from the µC. Because of this cheaper models can be in use for example.

3.4.1 Address Mapping Auto-increment mode

Address (bin)	*Size (Byte)*	*Access Type:*	*Description*	*Reset value*
00	1	w	Address (lower byte) Bit 7 .. 0 : Address bits 7 .. 0	-
01	1	w	Address (higher byte) Bit 7 .. 4 : Reserved Bit 3 .. 0 : Address bits 11 .. 8	-
10	1	w	Write Data Bit 7 .. 0 : Data bits 7 .. 0	-
10	1	r	Read Data Bit 7 .. 0 : Data bits 7 .. 0	00

Table 6: Address Mapping Auto Increment Mode

3.4.2 Software Handling Auto Increment Mode

Write

1. Write lower Byte of Address to register
2. Write higher Byte of Address to register
3. Write Data to register followed by auto-increment.

Read

4. Write lower Byte of Address to register
5. Write higher Byte of Address to register
6. Read Data from register followed by auto-increment.

3.4.3 Example Write

2 bytes on address 1234 (hex)

1. On address 00 (bin) write the data 34 (hex)
2. On address 01 (bin) write the data 12 (hex)
3. On address 10 (bin) write first byte
4. On address 10 (bin) write second byte

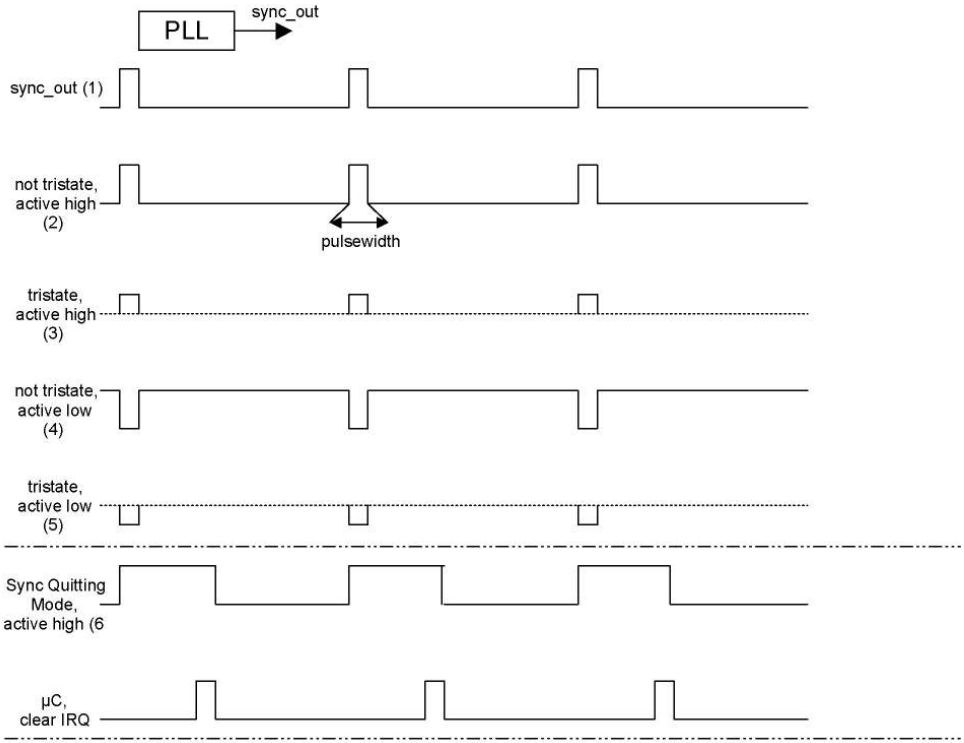
3.4.4 Example Read

4 bytes from address 5678 (hex)

1. On address 00 (bin) write the data 78 (hex)
2. On address 01 (bin) write the data 56 (hex)
3. On address 10 (bin) read first byte
4. On address 10 (bin) read second byte
5. On address 10 (bin) read third byte
6. On address 10 (bin) read fourth byte

3.5 Sync Modes

The Sync Mode Register offers the possibility to influence the synchronization behavior.



As can be seen in the figures 2 and 4 above there is the possibility to choose between active high and active low (Bit 1). Further the Sync Quitting Mode can be activated (Bit 0). In this mode the µC gives an acknowledge as can be seen in figure 6.
To prevent destruction of the output drivers there is the option to activate a tristate buffer (Bit 2) for the sync output (figures 3 and 5).
Bit 0 of the Sync Mode Register can also activate the Pulse Width Register. Values can be changed in steps of 20 ns.

3.6 Interrupt Output

The VEB 011C interrupt output can be configured over the same register as the Sync for low-active, high-active and/or tristate.
If an interrupt is triggered, the output is enabled and the interrupt source can then be determined in the VEB IRQ register. Possible sources are CANopen or EMAC, providing that these were previously activated in the VEB Interrupt Enable Register. The interrupt must be acknowledged in the respective register to deactivate the interrupt output (e.g. EMAC FIFO Status register – IRQ Quit register)

4 External Timing

4.1 Read

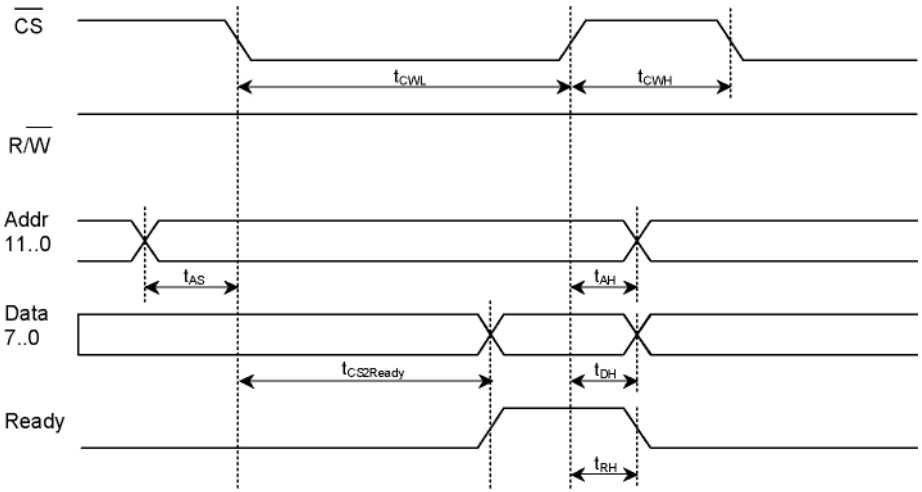


Figure 14: External Timing Read

4.2 Write

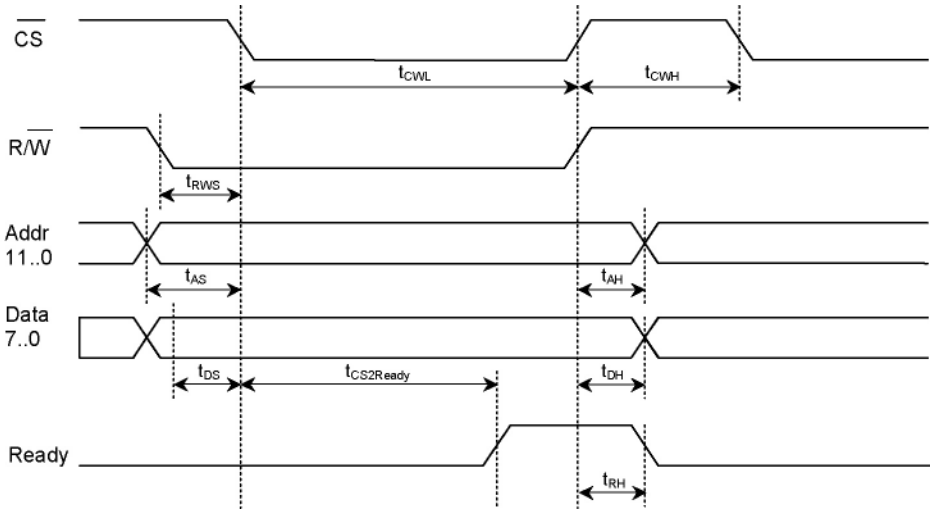


Figure 15: External Timing Write

5 Timing Characteristics

Timing	*Time (ns)*		*Description*
	min.	*max.*	
t_{CWL}	185	-	Chip select width low
t_{CWH}	40	-	Chip select width high
t_{RWS}	0	-	Read write setup time
t_{AS}	0	-	Address setup time
t_{DS}	0	-	Data setup time
t_{DH}	0	-	Data hold time
t_{AH}	0	-	Address hold time
t_{RH}	0	-	Ready hold time
$t_{CS2READY}$*	-	165	Chip select to ready time (fast) CANopen, DPRAM registers
$t_{CS2READY}$*	225	5345	Chip select to ready time (slow) VARAN control address space registers

Table 7: Timing Characteristics

***Attention: Delay time $t_{CS2READY}$ depends on accessed registers!**

6 List of Abbreviations

µC	Microcontroller
PDO	Process Data Object
SDO	Service Data Object
Mn	Manager
Cl	Client
MnPDO	Manager Process Data Object
MnSDO	Manager Service Data Object
ClPDO	Client Process Data Object
ClSDO	Client Service Data Object

VARAN Recommended Shielding

The VARAN real-time Ethernet bus system offers robust performance in harsh industrial environments. Through the use of IEEE 802.3 standard Ethernet physics, the potential between an Ethernet line and sending/receiving components is kept separate. The VARAN Manager resends messages to a bus participant immediately when an error occurs. It is principally recommended that the shielding guidelines below be followed.

For applications in which the bus line is run outside the control cabinet, correct shielding is required. This is especially important, if due to physical requirements, the bus lines must be placed next to sources of strong electromagnetic noise. It is recommended that whenever possible, to avoid wiring VARAN-Bus lines parallel to power cables.

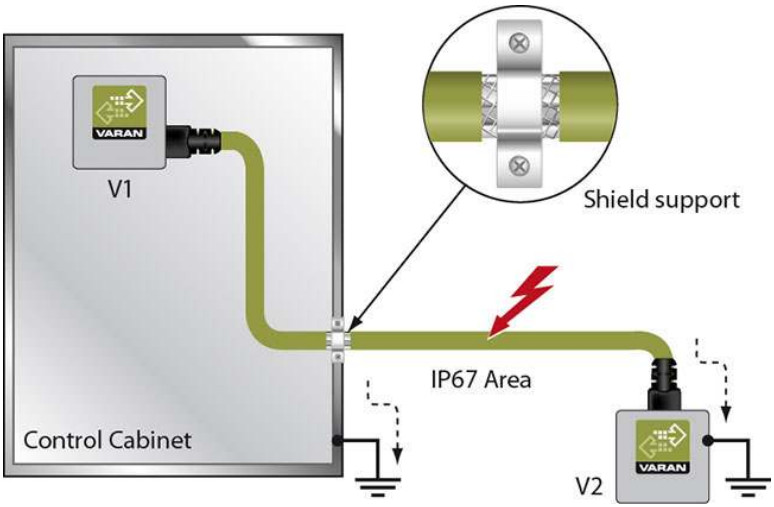
SIGMATEK recommends the use of **CAT5e** industrial Ethernet bus lines.

For the shielding variants, an S-FTP bus line is recommended, which is a symmetric, multi-wire cable with unshielded pairs. For the total shielding, a combination of foil and braiding is used; it is recommended that an unvarnished variant be used.

The VARAN cable must be secured at a distance of 20 cm from the connector for protection against vibration!

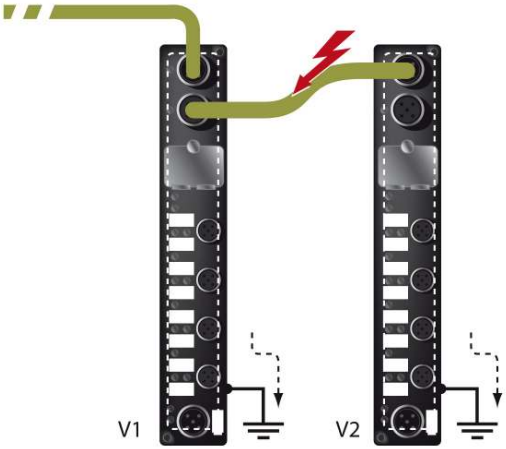
1. Wiring from the Control Cabinet to an External VARAN Component

If the Ethernet lines are connected from a VARAN component to a VARAN node outside the control cabinet, the shielding should be placed at the entry point to the control cabinet housing. All noise can then be deflected from the electronic components before reaching the module.



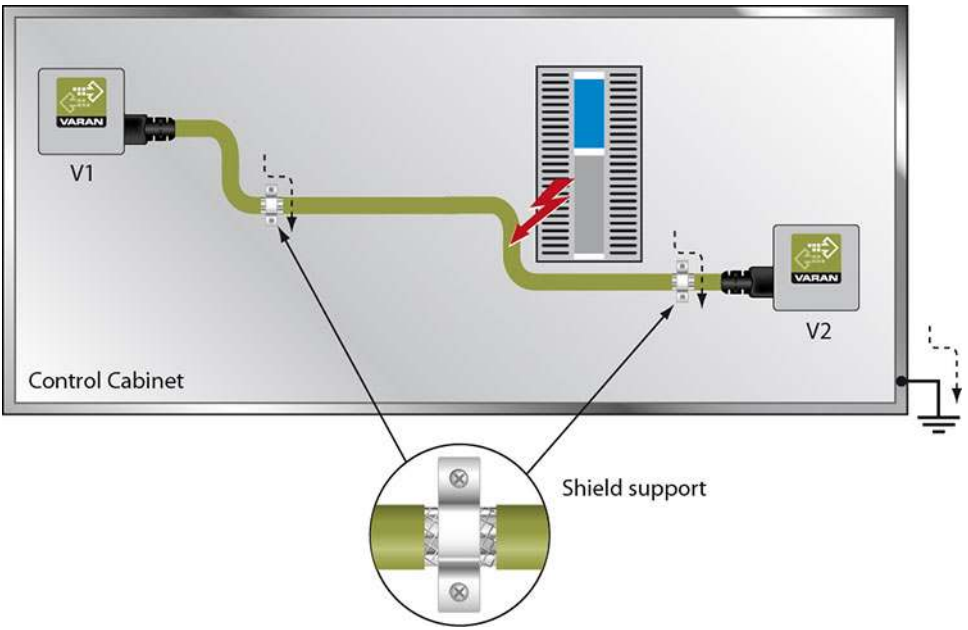
2. Wiring Outside of the Control Cabinet

If a VARAN bus cable must be placed outside of the control cabinet only, no additional shield connection is required. This requires that only IP67 modules and connectors be used. These components are very robust and noise resistant. The shielding for all sockets in IP67 modules are internally connected to common bus or electrically connected to the housing, whereby the deflection of voltage spikes does not flow through the electronics.



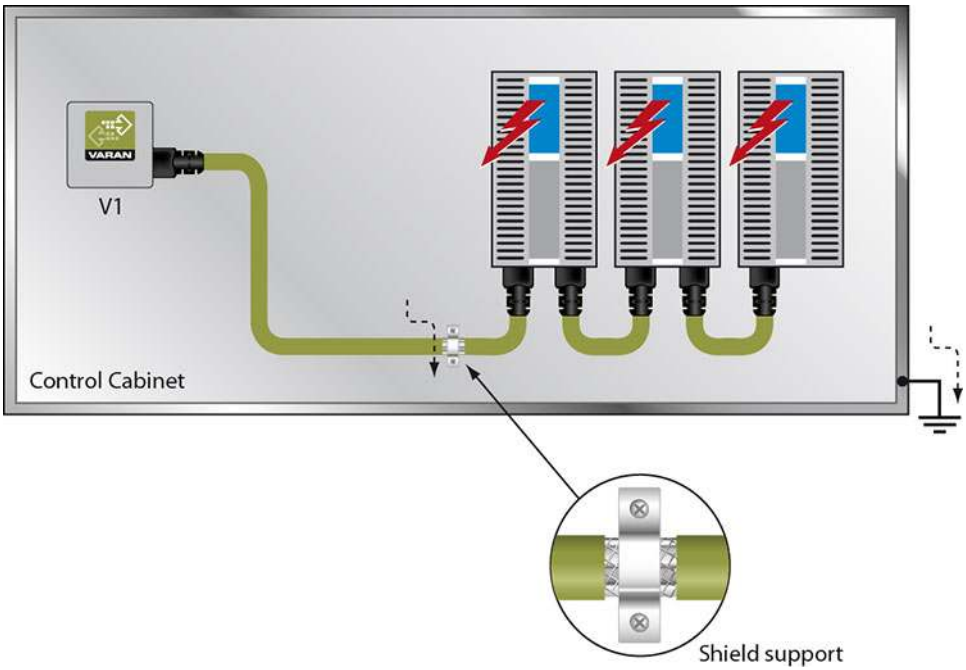
3. Shielding for Wiring Within the Control Cabinet

Sources of strong electromagnetic noise located within the control cabinet (drives, Transformers, etc.) can induce interference in a VARAN bus line. Spike voltages are deflected over the metallic housing of a RJ45 connector. Noise is conducted through the control cabinet housing without further action from the electronic components To eliminate sources of noise during data transfer, it is recommended that the shielding from all electronic components be connected within the control cabinet.



4. Connecting Noise-Generating Components

With the connection of power components that generate strong electromagnetic noise, it is also critical to ensure correct shielding. The shielding should be placed before a power component (or a group thereof).



5. Shielding Between Two Control Cabinets

If two control cabinets must be connected over a VARAN bus, it is recommended that the shielding be located at the entry points to both cabinets. Noise can thereby be kept from reaching the electronics within the control cabinet.