DM 162

S-DIAS Digital Mixed Module

Operating Manual

Date of creation: 27.02.2014 | Version date: 03.06.2022 | Article number: 20-008-162-E

Publisher: SIGMATEK GmbH & Co KG
A-5112 Lamprechtshausen
Tel.: +43/6274/4321
Fax: +43/6274/4321-18
Email: office@sigmatek.at
WWW.SIGMATEK-AUTOMATION.COM

Translation from German

S-DIAS Digital Mixed Module DM 162

with 4 digital inputs

4 digital inputs with counter function and time measurement

8 short-circuit proof digital outputs

The S-DIAS DM 162 digital mixed module has four digital inputs (+24 V/3.5 mA/5 ms), four digital inputs with counter function and time measurement and eight short-circuit proof digital outputs (+24 V/0.5 A). The supply voltage is monitored for under voltage.

Contents

1 Technical Data

1.1 Digital Input Specifications

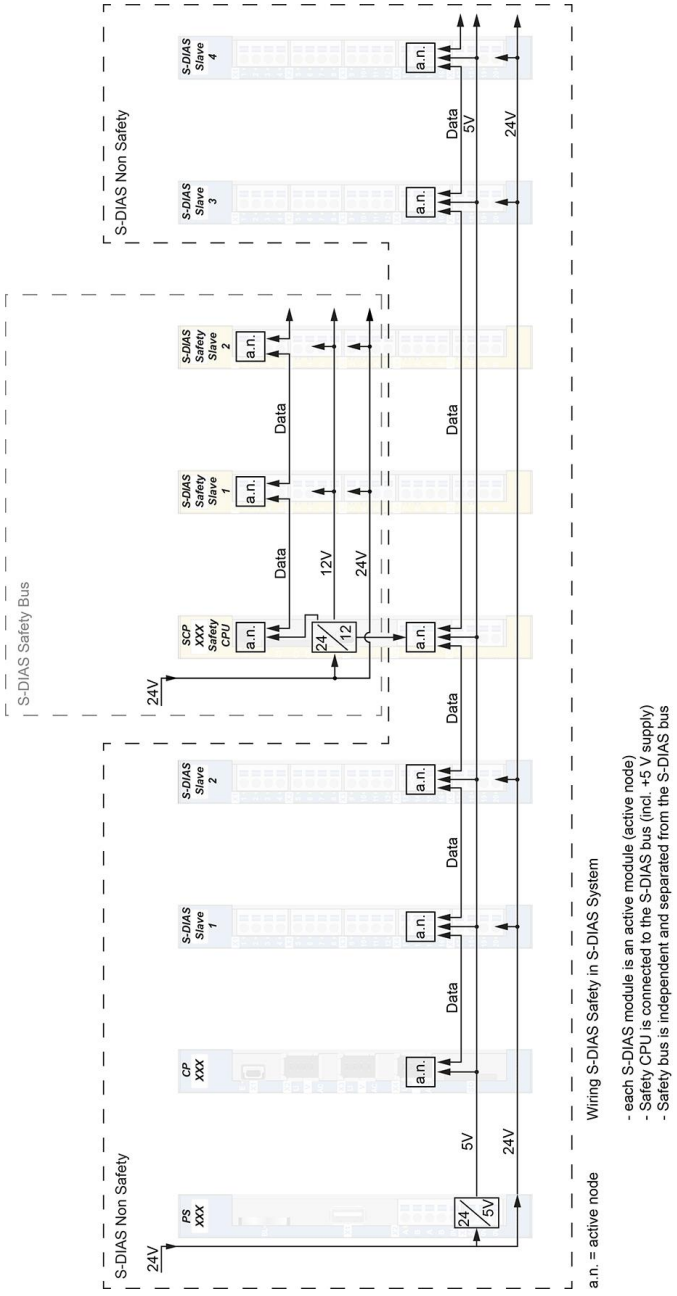
Number	8	
Input voltage	typically +24 V	maximum +30 V
Signal level (up to HW version 3.10)	low: < +8 V	high: > +14 V
Signal level (starting with HW version 3.20)	low: < +5 V	high: > +15 V
Input current	3.7 mA at +24 V	
Input delay	input 1-4: 1 µs (counter, time measurement) input 5-8: 5 ms	
Input frequency of counter input	25 kHz in normal counter mode or in incremental counter mode with 4-edge analysis	
Counter frequency	25 kHz in normal counter mode 100 kHz in incremental counter mode with 4-edge analysis	
Time measurement	measurement of the time between Sync and edge change in µsec for input 1-4	

1.2 Digital Output Specification

Number	8
Short-circuit proof	yes
Maximum continuous current load allowed per channel	0.5 A
Maximum total current (all 8 outputs)	4 A (100 % of on-time)
Maximum braking energy of outputs (inductive load)	maximum 1 Joule/channel
Residual current (off)	≤ 10 µA
Turn-on delay	< 100 µs (up to HW version 4.XX) < 200 µs (starting with HW version 5.00)
Turn-off delay	< 150 µs (up to HW version 4.XX) < 200 µs (starting with HW version 5.00)

1.3 Electrical Requirements

Power supply +24 V	18-30 V DC	
Current consumption of the +24 V supply	corresponds to the load on the digital outputs	
Voltage supply from S-DIAS bus	+5 V	
Current consumption on the S-DIAS bus (+5 V supply)	typically 50 mA	maximum 55 mA


S-DIAS Non Safety
24V
PS XXX
CP XXX
S-DIAS Slave 1
S-DIAS Slave 2
a.n.
Data
5V
24V
24/5V
S-DIAS Safety Bus
SCP XXX Safety CPU
S-DIAS Safety Slave 1
S-DIAS Safety Slave 2
12V
24/12
S-DIAS Non Safety
S-DIAS Slave 3
S-DIAS Slave 4
a.n. = active node
Wiring S-DIAS Safety in S-DIAS System
- each S-DIAS module is an active module (active node)
- Safety CPU is connected to the S-DIAS bus (incl. +5 V supply)
- Safety bus is independent and separated from the S-DIAS bus

1.4 Voltage Monitor

Power supply +24 V	Supply voltage > 18 V (DC OK-LED lights green)

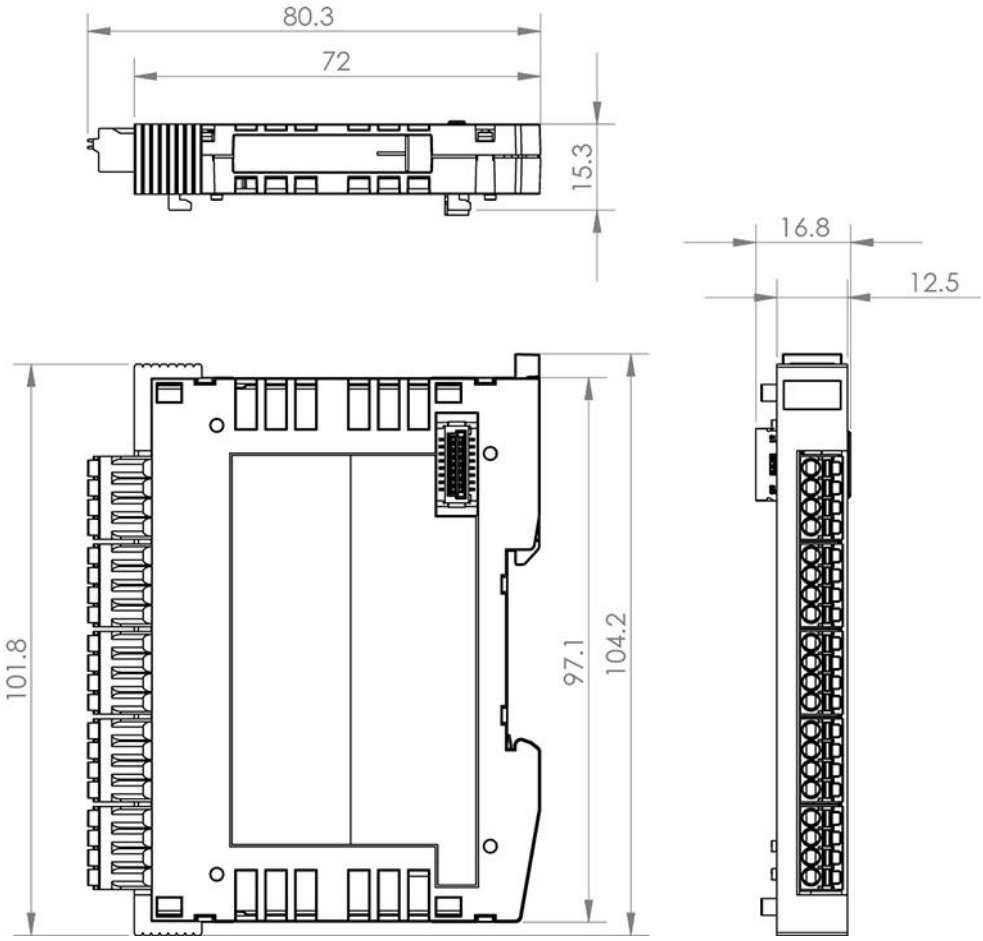
1.5 Miscellaneous

Article number	20-008-162
Hardware version	1.x-6.x
Standard	UL 508 (E247993)
Approbations	UL, cUL, CE

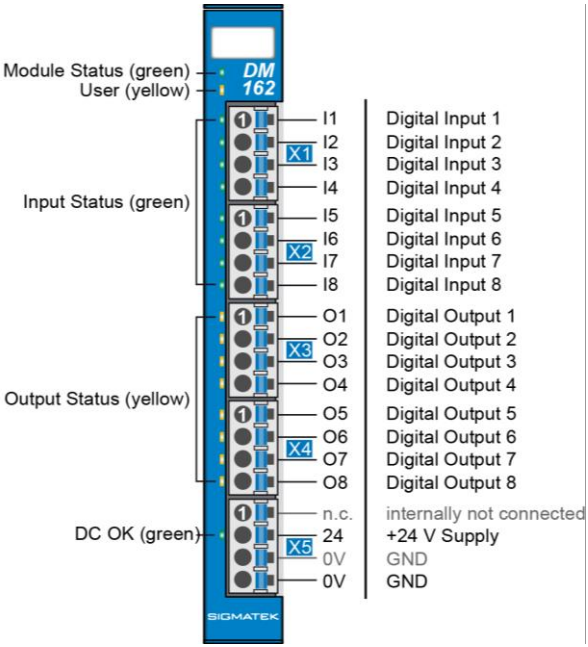
1.6 Environmental Conditions

Storage temperature	-20 ... +85 °C	
Environmental temperature	0 ... +60 °C	
Humidity	0-95 %, non-condensing	
Installation altitude above sea level	0-2000 m without derating > 2000 m with derating of the maximum environmental temperature by 0.5 °C per 100 m	
Operating conditions	Pollution degree 2	
EMC resistance	in accordance with EN 61000-6-2 (industrial area)	
EMC noise generation	in accordance with EN 61000-6-4 (industrial area)	
Vibration resistance	EN 60068-2-6	3.5 mm from 5-8.4 Hz 1 g from 8.4-150 Hz
Shock resistance	EN 60068-2-27	15 g
Protection type	EN 60529	IP20

2 Mechanical Dimensions



3 Connector Layout



The pins 3 & 4 of the connector X5 are bridged within the module. For the GND supply of the module only the connection of pin 4 is necessary. The internally bridged connections may be used for further looping of the GND supply. However, it must be taken into account that a total current of 6 A per connection is not exceeded as a result of further looping!

3.1 Status LEDs

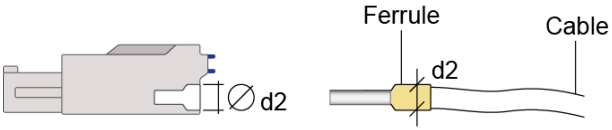
Module Status	green	ON	module active
		OFF	no supply available
		BLINKING (5 Hz)	no communication
User	yellow	ON	can be set from the application (e.g. the module LED can be set to blinking through the visualization so that the module is easily found in the control cabinet)
		OFF	
		BLINKING (2 Hz)	
		BLINKING (4 Hz)	
Input Status	green	ON	input ON
		OFF	input OFF
Output Status	yellow	ON	output on
		OFF	output off
DC OK	green	ON	voltage is supplied to the output group

3.2 Applicable Connectors

Connectors:
X1-X5: Connectors with spring terminals (included in delivery)
The spring terminals are suitable connecting ultrasonically compacted (ultrasonically welded) strands.

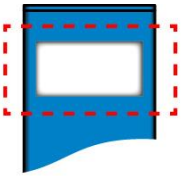
Connections:

Stripping length/Sleeve length:	10 mm
Mating direction:	parallel to the conductor axis or circuit board
Conductor cross section rigid:	0.2-1.5 mm^2
Conductor cross section flexible:	0.2-1.5 mm^2
Conductor cross section ultrasonically compacted:	0.2-1.5 mm^2
Conductor cross section AWG/kcmil:	24-16
Conductor cross section flexible with ferrule without plastic sleeve:	0.25-1.5 mm^2
Conductor cross section flexible with ferrule with plastic sleeve:	0.25-0.75 mm^2 (reason for reduction d2 of the ferrule)



d2 = max. 2.8 mm

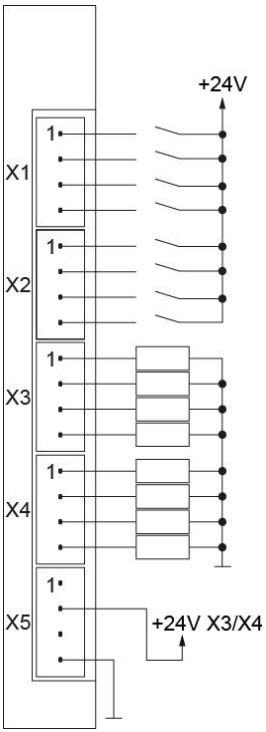
3.3 Label Field



Manufacturer	Weidmüller
Type	MF 10/5 CABUR MC NE WS
Weidmüller article number	1854510000
Compatible printer	Weidmüller
Type	Printjet Advanced 230V
Weidmüller article number	1324380000

4 Wiring

4.1 Wiring Example



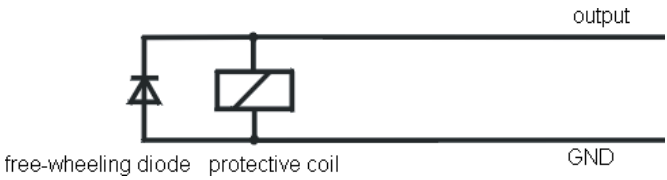
4.2 Note

- Up to 8 outputs are powered by a common +24 V supply.
- The cross section of the conductor for the +24 supply must be sufficient for the maximum total current.
- The outputs can be turned off by turning off the +24 V supply voltage.
- Applying power to an output whose supply voltage exceeds 0.7 V is not allowed.

Inductive loads must always be connected to a freewheeling diode or an RC network. This should be placed as close to the load as possible.

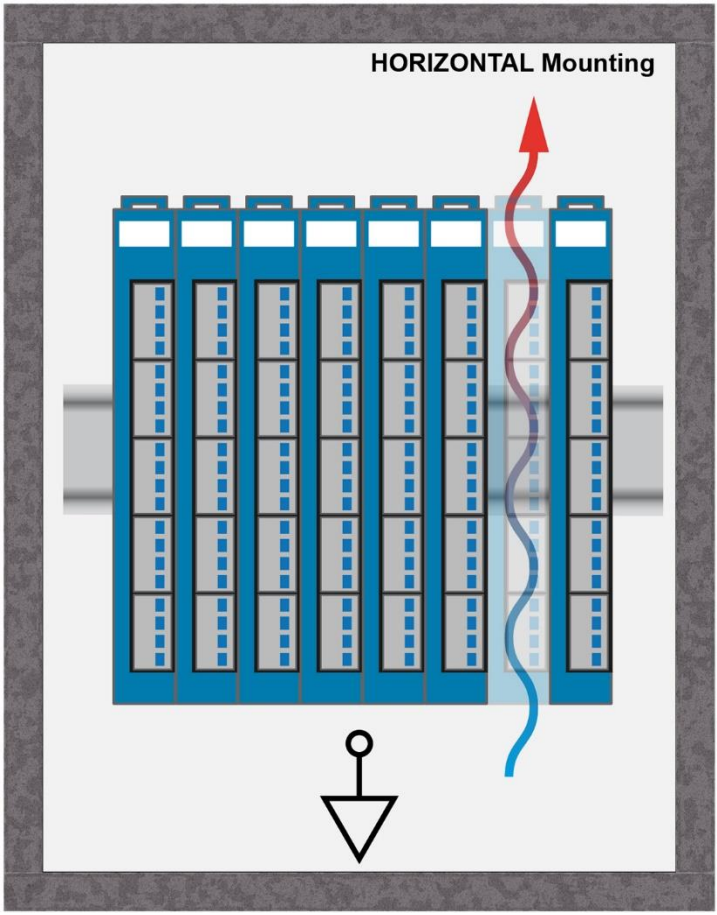
IMPORTANT:
The S-DIAS module CANNOT be connected/disconnected while voltage is applied!

4.2.1 Connecting Inductive Loads

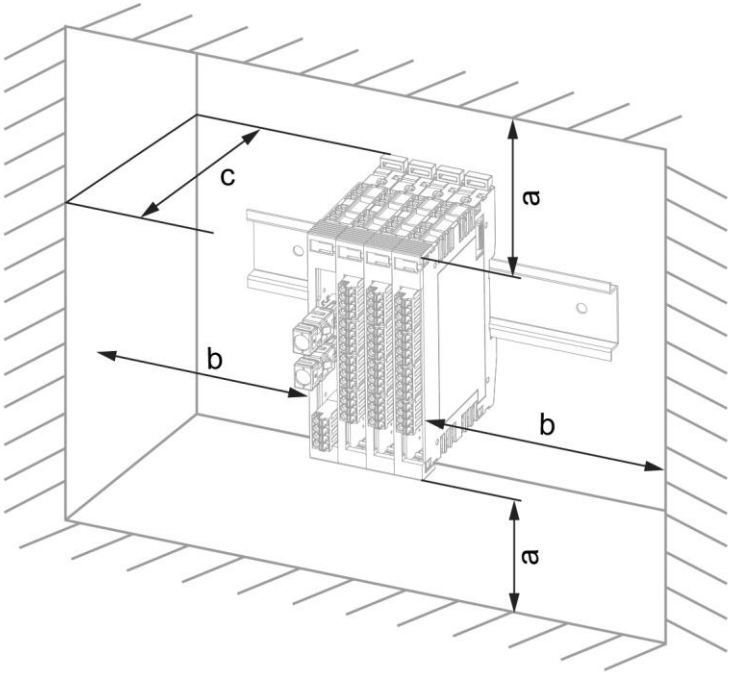


5 Mounting

The S-DIAS modules are designed for installation into the control cabinet. To mount the modules a DIN-rail is required. The DIN rail must establish a conductive connection with the back wall of the control cabinet. The individual S-DIAS modules are mounted on the DIN rail as a block and secured with latches. The functional ground connection from the module to the DIN rail is made via the grounding clamp on the back of the S-DIAS modules. The modules must be mounted horizontally (module label up) with sufficient clearance between the ventilation slots of the S-DIAS module blocks and nearby components and/or the control cabinet wall. This is necessary for optimal cooling and air circulation, so that proper function up to the maximum operating temperature is ensured.



Recommended minimum distances of the S-DIAS modules to the surrounding components or control cabinet wall:



a	b	c
30 mm (1.18˝)	**30 mm** (1.18˝)	**100 mm** (3.94˝)

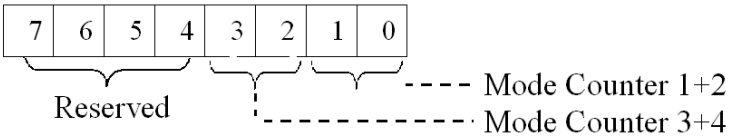
a, b, c … distances in mm (inches)

6 Description of the Counters

Four modes for the configuration of the counters are available:

1. Each rising edge on input n is counted. Counter 1 counts Input 1, Counter 2 counts Input 2, etc.
2. Counter for incremental encoder, four edge detection
3. Time stamp mode
4. PWM signal measurement (high-time and period)

Counter mode register 1:



Each setting is assigned to two counters

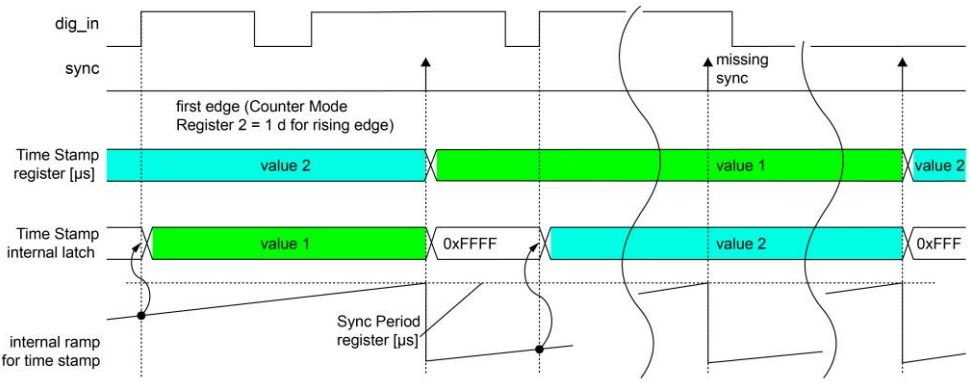
Mode = 0: Normal edge counter for rising edges
Mode = 1: Incremental encoder counter (e.g. input 1 > channel A and input 2 > channel B). Depending on rotation direction the counter counts up or down. Resetting the counters is not possible.
Mode = 2: Time stamp mode. A µs time stamp in relation to the S-DIAS sync is read on the defined edge (Reg. 0x0001).
Mode = 3: PWM signal measurement. Measures period and high time with a fixed resolution of 1 µs. No prescaling possible.

The Counter Mode Register 2 is used to set the edge detection for each digital input (latch input).

Set register “Counter Mode Register 1” and “Counter Mode Register 2” at start-up during initialization. Do not use in cyclic data, else the latch registers are reset!

6.1 Time Stamp Mode

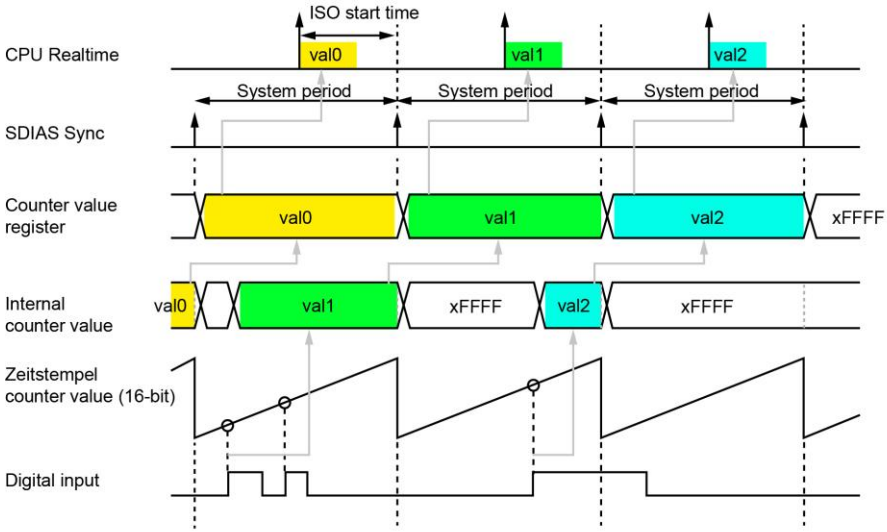
The timestamp value represents the latch of the internal time stamp latch register. On occurring sync the register is latched. An internal ramp counter counts, until it reaches the value of Sync Period register, or until a sync occurs. On the first rising or first falling edge of the “latch” input (dig_in) the recent counter value is stored in the internal time stamp latch register according to the input. Edge detection depends on “Counter Mode Register 2” settings.

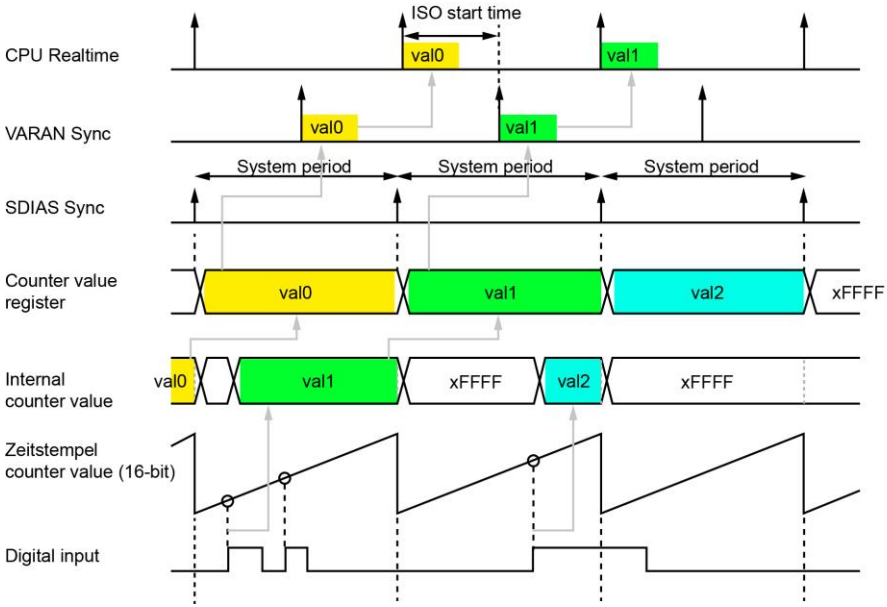


In the design no interpolation of the sync exists. The “Sync Period” register is the reset value for the internal ramp counter. At start up the system period of the incoming sync must be written to the Sync Period register. Default value is 1 ms (0x03E8 = 1000 µs). If the internal ramp counter reaches the value of Sync Period register the counter resets. Hence on missing sync the counter will not overflow.
If no valid edge was detected, during the previous system period, the register contains the value 0xFFFF.
The latch registers are reset when “Counter Mode Register 1” or “Counter Mode Register 2” is written.

6.1.1 Example Edge Mode with Rising Edge

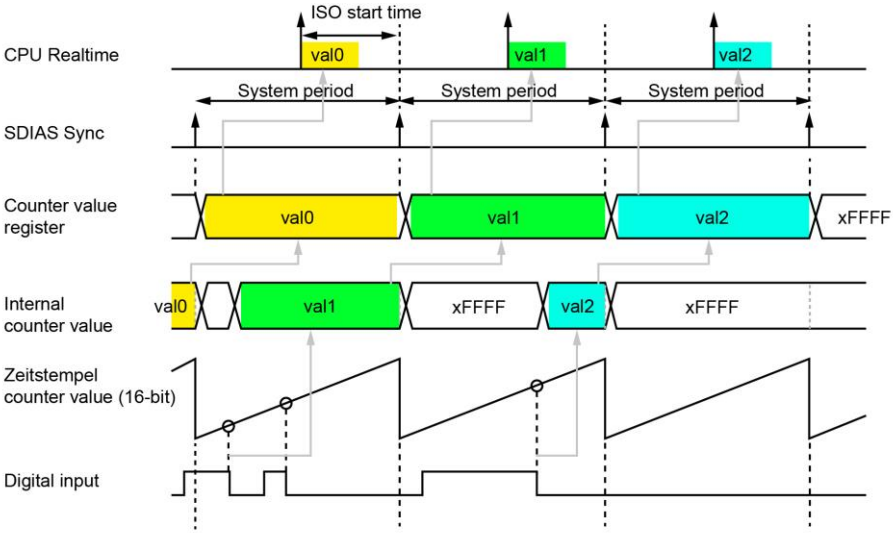
1. graphic with local S-DIAS bus, 2. graphic S-DIAS bus behind VARAN

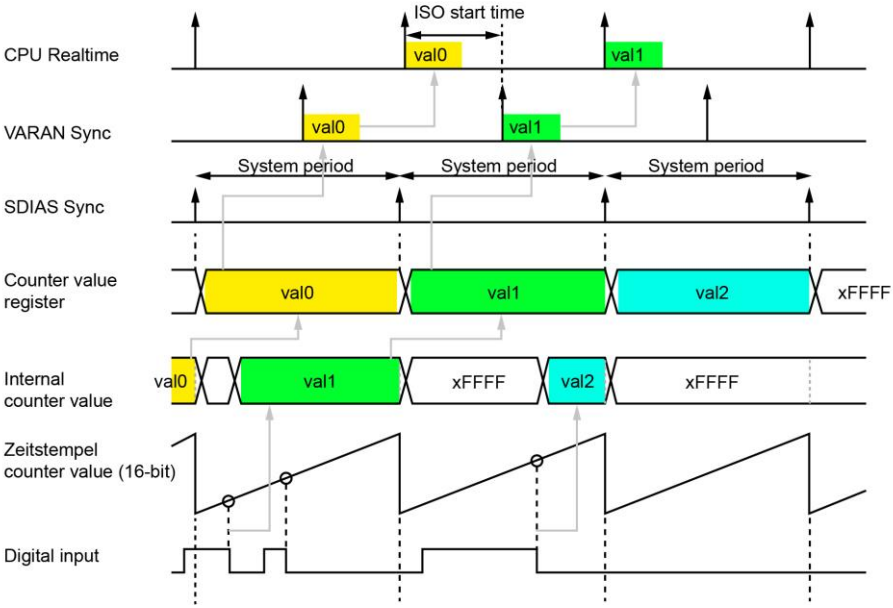




6.1.2 Example Edge Mode with falling edge

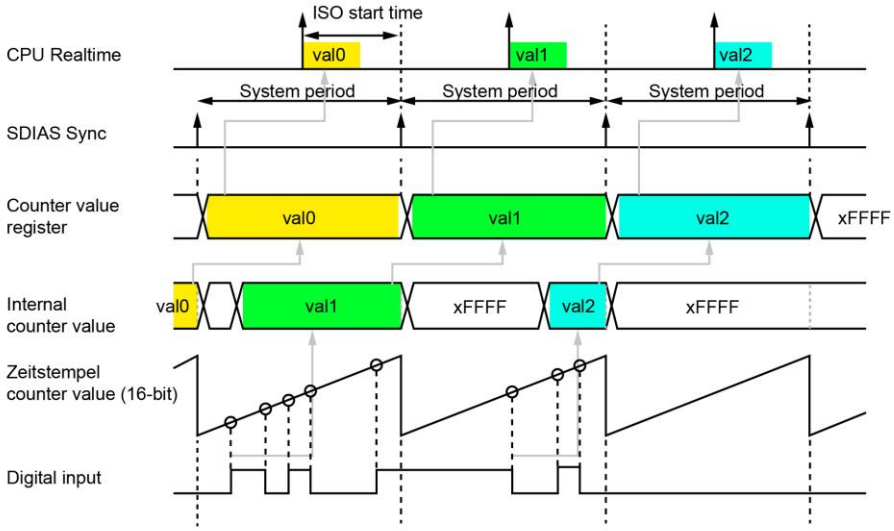
1. graphic with local S-DIAS bus, 2. graphic S-DIAS bus behind VARAN

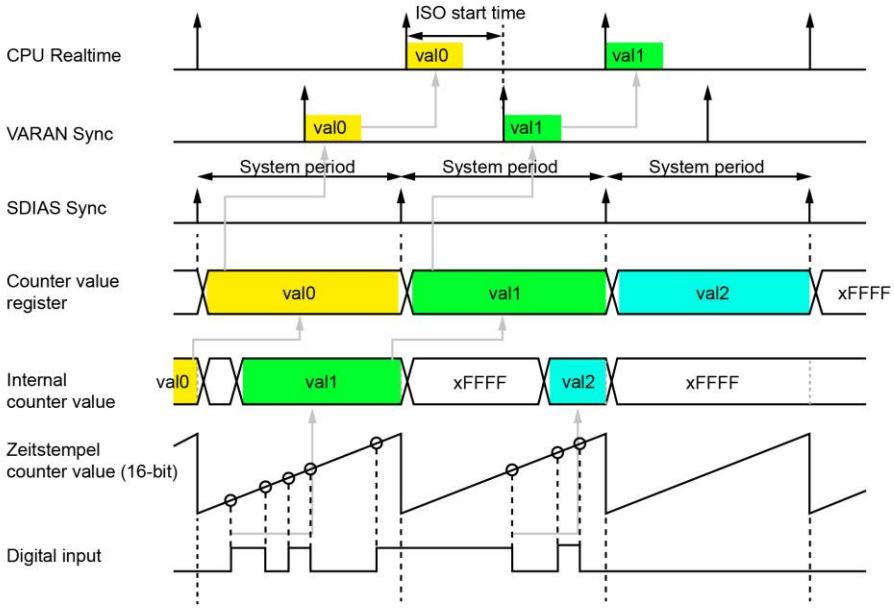




6.1.3 Example Edge Mode with both edges

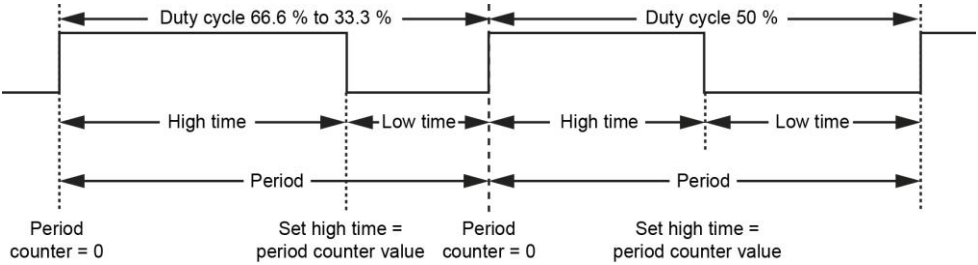
1. graphic with local S-DIAS bus, 2. graphic S-DIAS bus behind VARAN



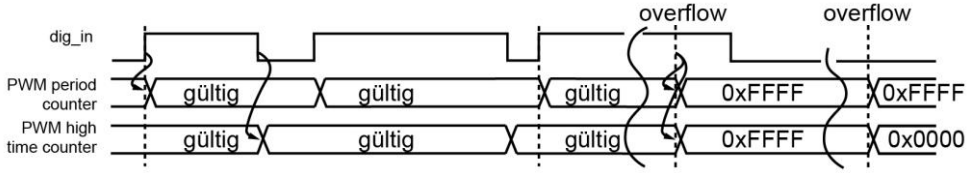


6.2 PWM Signal Measurement

This mode supports measurements on the inputs 1 to 4. The counter value for period and high time is displayed in µs.



The period measures the elapsed time between the rising edges of the digital input (dig_in). On the first rising edge of dig_in a counter starts to increment each µs. On the second rising edge of dig_in the counter value is latched by the corresponding “PWM period counter” register. The counter resets after latching the value.



The same counter is used to measure the high time of dig_in. On falling edge of dig_in the recent counter value is stored in the “PWM high time counter” register.
At counter overflow the “PWM period counter” register value is 0xFFFF. The value of the “PWM high time counter” register, when counter overflows, depends on the dig_in input level. On high-level the register returns the value 0xFFFF, on low-level the value is 0x0000.

7 Addressing

Address (hex)	Size (bytes)	Access Type	Description	Reset value
Memory				
0000	1	r/w	Counter mode register 1 (1) Bit 0-1 Counter mode 1+2 Bit 2-3 Counter mode 3+4 Bit 4-7 reserved (0 = normal counter mode, 1 = incremental counter mode, 2 = timestamp mode, 3 = PWM measuring mode)	0000
0001	1	r/w	Counter mode register 2 (1) Bit 0-1 Select edge for timestamp mode cnt 1 Bit 2-3 Select edge for timestamp mode cnt 2 Bit 4-5 Select edge for timestamp mode cnt 3 Bit 6-7 Select edge for timestamp mode cnt 4 (0 = no edge selected, 1= rising edge, 2 = falling edge, 3 = both edges)	0000
0002	2	w16	Sync period (system period) Sync period in µs	03E8
0004	1	w	Output register Bit 0 Output 1 Bit 1 Output 2 … Bit 7 Output 8	00
0004	1	r	Input register Bit 0 Input 1 Bit 1 Input 2 … Bit 7 Input 8	00
0005	1	r	24 V status Bit 0 DC 24 V OK Bit 1-7 reserved	01
0006	1	r	Counter 1 (2) 8-bit counter for input 1	00
0006	2	r16	Incremental encoder 1 (3) 16-bit incremental encoder counter	0000

0006	2	r16	Time stamp input 1 [resolution: 1 µs] (4) 16-bit counter	FFFF
0006	2	r16	PWM high time counter for input 1 [resolution: 1 µs] (5) 16-bit counter, value of the counter for falling edge of input 1	FFFF
0007	1	r	Counter 2 (2) 8-bit counter for input 2	00
0008	1	r	Counter 3 (2) 8-bit counter for input 3	00
0008	2	r16	Incremental encoder 2 (3) 16-bit incremental encoder counter	0000
0008	2	r16	Time stamp input 3 [resolution: 1 µs] (4) 16-bit counter	FFFF
0008	2	r16	PWM high time counter for input 3 [resolution: 1 µs] (5) 16-bit counter, value of the counter for falling edge of input 3	FFFF
0009	1	r	Counter 4 (2) 8-bit counter for input 4	00
000A	2	r16	Time stamp input 2 [resolution: 1 µs] (4) 16-bit counter	FFFF
000A	2	r16	PWM high time counter for input 2 [resolution: 1 µs] (5) 16-bit counter, value of the counter for falling edge of input 2	FFFF
000C	2	r16	Time stamp input 4 [resolution: 1 µs] (4) 16-bit counter	FFFF
000C	2	r16	PWM high time counter for input 4 [resolution: 1 µs] (5) 16-bit counter, value of the counter for falling edge of input 4	FFFF
000E	2	r16	PWM period counter for input 1 [resolution: 1 µs] (5) 16-bit counter	0000
0010	2	r16	PWM period counter for input 2 [resolution: 1 µs] (5) 16-bit counter	0000

0012	2	r16	PWM period counter for input 3 [resolution: 1 µs] (5) 16-bit counter	0000
0014	2	r16	PWM period counter for input 4 [resolution: 1 µs] (5) 16-bit counter	0000

(1) Writing to this register clears all counter values (if performed during the count process, the first edge could be missed).
(2) If the mode register for the counter mode is set.
(3) If the mode register is set for the incremental encoder mode.
(4) If the mode register is set for the time stamp mode.
(5) If the mode register is set for the PWM mode.

8 Supported Cycle Times

8.1 Cycle Times below 1 ms (in µs)

50	100	125	200	250	500
x	x	x	x	x	x

x= supported

8.2 Cycle Times equal to or higher than 1 ms (in ms)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

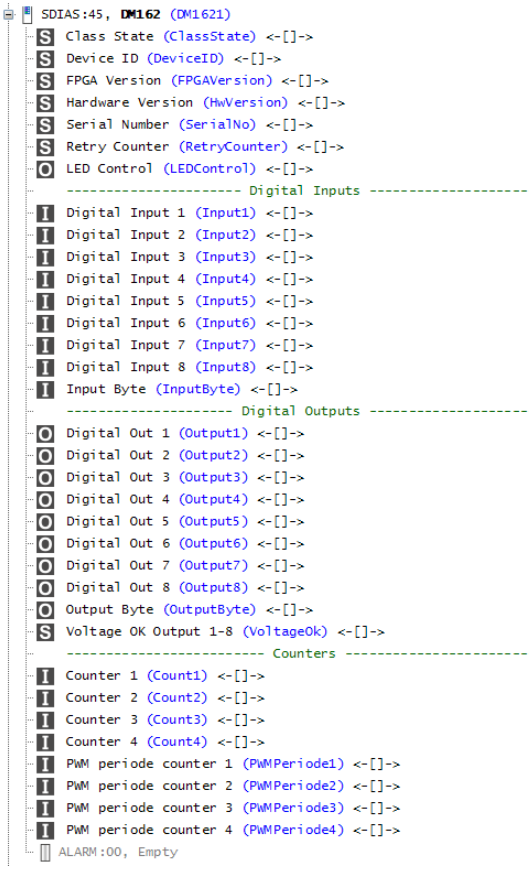
x= supported

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x= supported

9 Hardware Class DM162

Hardware Class DM162 for the S-DIAS DM162 digital module



This hardware class is used to control the DM 162 hardware module with 8 digital outputs and 8 digital inputs. Of the 8 inputs, the first 4 can be used as counters, for time measurement or to measure a PWM signal. More information on the hardware can be found in the module documentation.

9.1 Interfaces

9.1.1 Clients

SdiasIn	The client must be connected to an S-DIAS port, an "SdiasOut"_[x]" server.
Place	The physical location of the hardware module is entered in this client. Up to 64 modules, 0 to 63, can be assigned.
Required	This client is active by default, which means that the S-DIAS hardware module at this position is mandatory for the system and can under no circumstances be disconnected or return an error. Otherwise, the entire hardware deactivated. If the hardware module is missing or removed, an S-DIAS error is triggered. If his client is initialized with 0, the hardware module located in this position is not mandatory. This means that it doesn't have to be available or error-free. However, which components identified as "not required" should be selected with regard to the safety of the system.
CountMode[1,2]	Counter setting 1 or 2 as an initialization value: 0 – no counter 1 – counter counts with a signal from Input1 and Input2 or Input3 and Input 4 2 – incremental encoder (Input1 and Input2 or Input3 and Input4) 3 – time mode (Input1 and Input2 or Input3 and Input4) 4 – PWM signal measuring module (Input1 and 2 or Input3 and 4)
EdgeMode[1-4]	Setting for the Edge time measurement of inputs 1-4 as an initialization value. Used only when CountMode is set to time measuring for the respective channel (Countmode = 3). 0 – time measurement edge disabled 1 – Sync until the first positive edge of the period 2 – Sync until the firs negative edge of the period 3 – Sync until the first positive or negative edge of the period

9.1.2 Servers

ClassState	This server shows the actual status of the hardware class.
DeviceID	The device ID of the hardware module is shown in this server.
FPGAVersion	FPGA version of the module in 16#XY (e.g. 16#10 = version 1.0).
SerialNo	The serial number of the hardware module is shown in this server.
RetryCounter	This server increments when a transfer fails.
LEDControl	With this server, the application LED of the S-DIAS module can be activated to find the module in the network more quickly. The following statuses are possible: 0 – LED off 1 – LED on 2 – Blinks slowly 3 – Blinks rapidly
Input[1-8]	Status of input 1-8
Output[1-8]	Output 1-8, Output set via the write() method.

InputByte	In this server, the digital outputs are shown in an 8-bit field. Within this bit field, 0 to 7 are allocated to inputs input1 to input8
OutputByte	In this server, the digital outputs are shown in a 8-bit field. In this word, bits 0 to 7 are allocated to output1 to output8. A write() instruction to this server writes the bit pattern to these outputs.
Count[1-4]	The displayed values are dependent on the client setting of CountMode. CountMode[1,2]: 0 disabled 1 normal counter input 1,2 or 3,4 2 incremental encoder input 1,2 or 3,4 whereby the server Count2 or Count4 is disabled. 3 time measurement for input 1,2 or 3,4 in µs If now edge occurs, this server shows 65535. 4 PWM turn-on time for input 1,2 or 3,4 in µs If the input is continuously on, this server shows 65535. Count can be reset with the write method of the server.
PWMPeriode[1-4]	The displayed values are dependent on the client setting of CountMode. CountMode[1,2]: 0-3 Server is deactivated 4 PWM period for input 1,2 or 3,4 in µs If no period is detected, this server shows 65535.
VoltageOk	The voltage supply for outputs 1-8 is displayed in this server. 0 power supply error 1 power supply ok

9.1.3 Communication Interfaces

ALARM	Downlink	With this downlink the corresponding alarm class can be placed via the hardware editor.

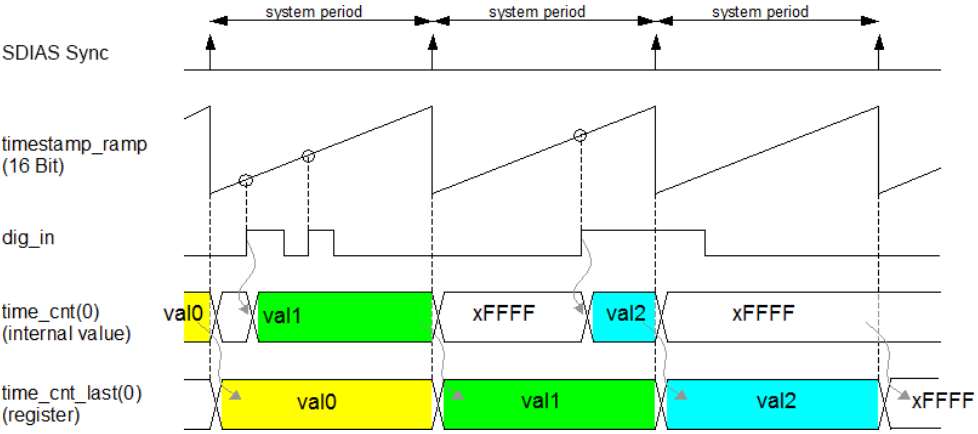
9.2 Main Display of the Time Measuring Function

This function can be used for inputs 1-4. The Countmode[1,2] = 3 setting is therefore required. In the diagram below, the response of EdgeMode 1-3 is shown.

Depending on the mode setting, the time until the first edge is measured in µs. If now edge occurs, the server shows the value 65535.

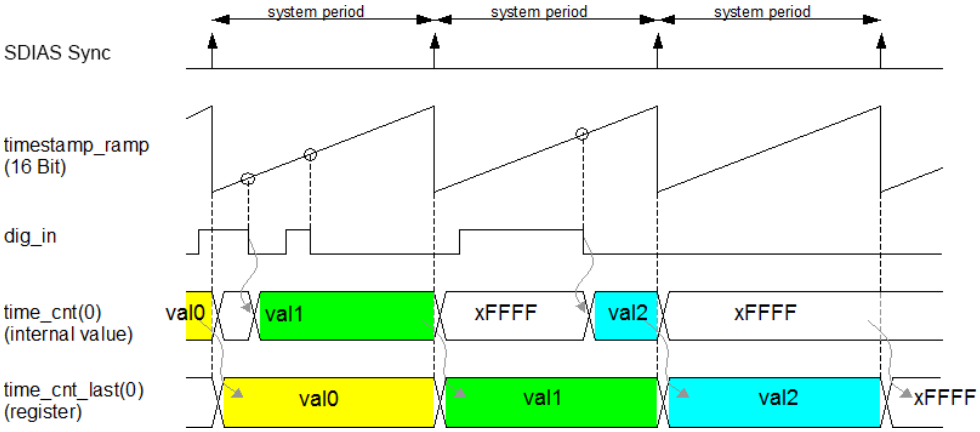
9.2.1 EdgeMode = 1

Time is measured from Sync to the first positive edge.



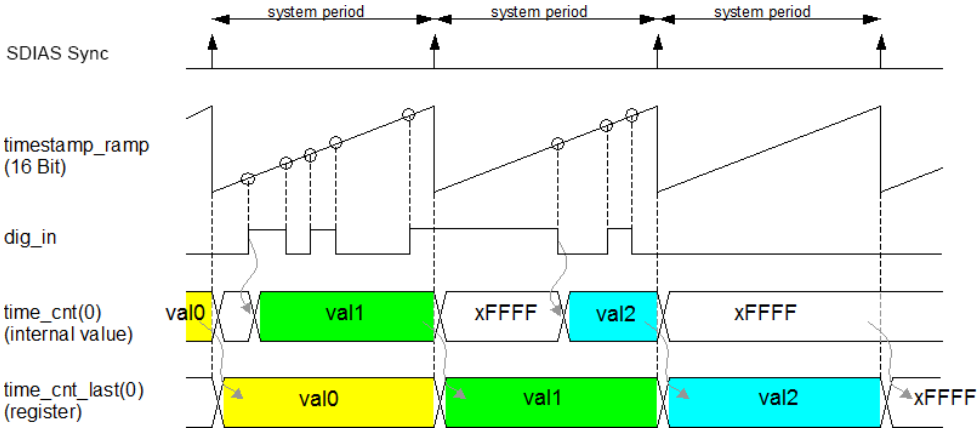
9.2.2 EdgeMode = 2

Time is measured from Sync to the first negative edge.



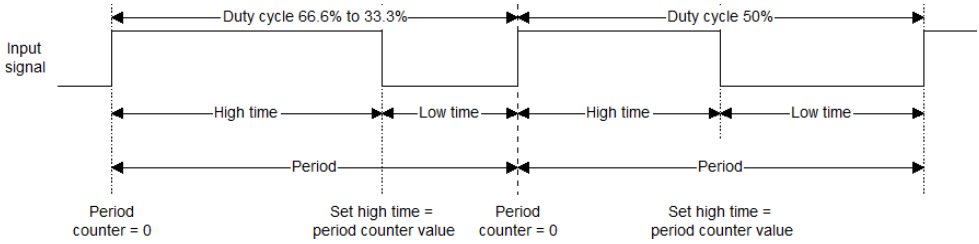
9.2.3 EdgeMode = 3

Time is measured from Sync to the first positive or negative edge.

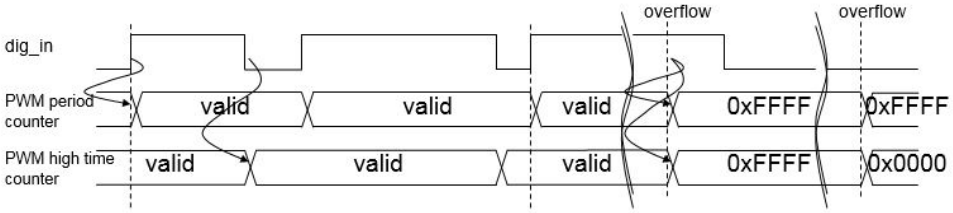


9.3 Main Display of the PWM Measuring Function

This function can be used for inputs 1-4. The Countmode[1,2] = 4 setting is therefore required. A count register is available for the period (PWMPeriod[1-4]) and for the turn on time (Count[1-4]) in µs. If the turn on time is 100 % of the period, 65535 is displayed in the Count[1-4] server.



The period is measured the elapsed time between the rising edges of the digital input (dig_in). On the first rising edge of dig_in a counter starts to increment each µs. On the second rising edge of dig_in the counter value is latched by the corresponding “PWM period counter” register. The counter resets after latching the value.



The same counter is used to measure the high time of dig_in. On falling edge of dig_in the recent counter value is stored in the “PWM high time counter” register.
At counter overflow the “PWM period counter” register value is 0xFFFF. The value of the “PWM high time counter” register, when counter overflows, depends on the dig_in input level. On high-level the register returns the value 0xFFFF, on low-level the value is 0x0000.

9.3.1 Detailed Address Mapping

Address (hex)	Size (Byte)	Access Type	Description	Reset value
Memory				
0000	1	r/w	Counter Mode Register 11) Bit 1..0: Mode Counter 1+2 Bit 3..2: Mode Counter 3+4 Bit 7..4: Reserved (0 = Normal counter mode, 1 = Incremental counter mode, 2 = Time Stamp mode, 3 = PWM Measure Mode)	0000
0001	1	r/w	Counter Mode Register 21) Bit 1..0: Edge select for time stamp mode Cnt 1 Bit 3..2: Edge select for time stamp mode Cnt 2 Bit 5..4: Edge select for time stamp mode Cnt 3 Bit 7..6: Edge select for time stamp mode Cnt 4 (0 = no edge selected, 1= rising edge, 2 = falling edge, 3 = both edges)	0000
0002	2	w16	Sync Period (System Period) Sync Period in µs	03E8
0004	1	w	Output Register Bit 0: Output 1 Bit 1: Output 2 … Bit 7: Output 8	00
0004	1	r	Input Register Bit 0: Input 1 Bit 1: Input 2 … Bit 7: Input 8	00
0005	1	r	24 V Status Bit 0: DC 24 V OK Bit 7..1: Reserved	01
0006	1	r	Counter 12) 8 Bit Counter for input 1	00
0006	2	r16	Incremental Encoder 13) 16 Bit Encoder Counter	0000
0006	2	r16	Time Stamp Input 1 [1µs]4) 16 Bit Counter	FFFF
0006	2	r16	PWM high time counter for input 1 [1µs]5) 16 Bit Counter, value of latched period counter 1 at falling edge of input 1	FFFF
0007	1	r	Counter 22) 8 Bit Counter for input 2	00
0008	1	r	Counter 32) 8 Bit Counter for input 3	00
0008	2	r16	Incremental Encoder 23) 16 Bit Encoder Counter	0000

0008	2	r16	Time Stamp Input 3 [1µs]4) 16 Bit Counter	FFFF
0008	2	r16	PWM high time counter for input 3 [1µs]5) 16 Bit Counter, value of latched period counter 3 at falling edge of input 3	FFFF
0009	1	r	Counter 42) 8 Bit Counter for input 4	00
000A	2	r16	Time Stamp Input 2 [1µs]4) 16 Bit Counter	FFFF
000A	2	r16	PWM high time counter for input 2 [1µs]5) 16 Bit Counter, value of latched period counter 2 at falling edge of input 2	FFFF
000C	2	r16	Time Stamp Input 4 [1µs]4) 16 Bit Counter	FFFF
000C	2	r16	PWM high time counter for input 4 [1µs]5) 16 Bit Counter, value of latched period counter 4 at falling edge of input 4	FFFF
000E	2	r16	PWM period counter for input 1 [1µs]5) 16 Bit Counter	0000
0010	2	r16	PWM period counter for input 2 [1µs]5) 16 Bit Counter	0000
0012	2	r16	PWM period counter for input 3 [1µs]5) 16 Bit Counter	0000
0014	2	r16	PWM period counter for input 4 [1µs]5) 16 Bit Counter	0000

1) Writing this register clears all counter values (The first edge maybe missing, if this is done during counting process.)

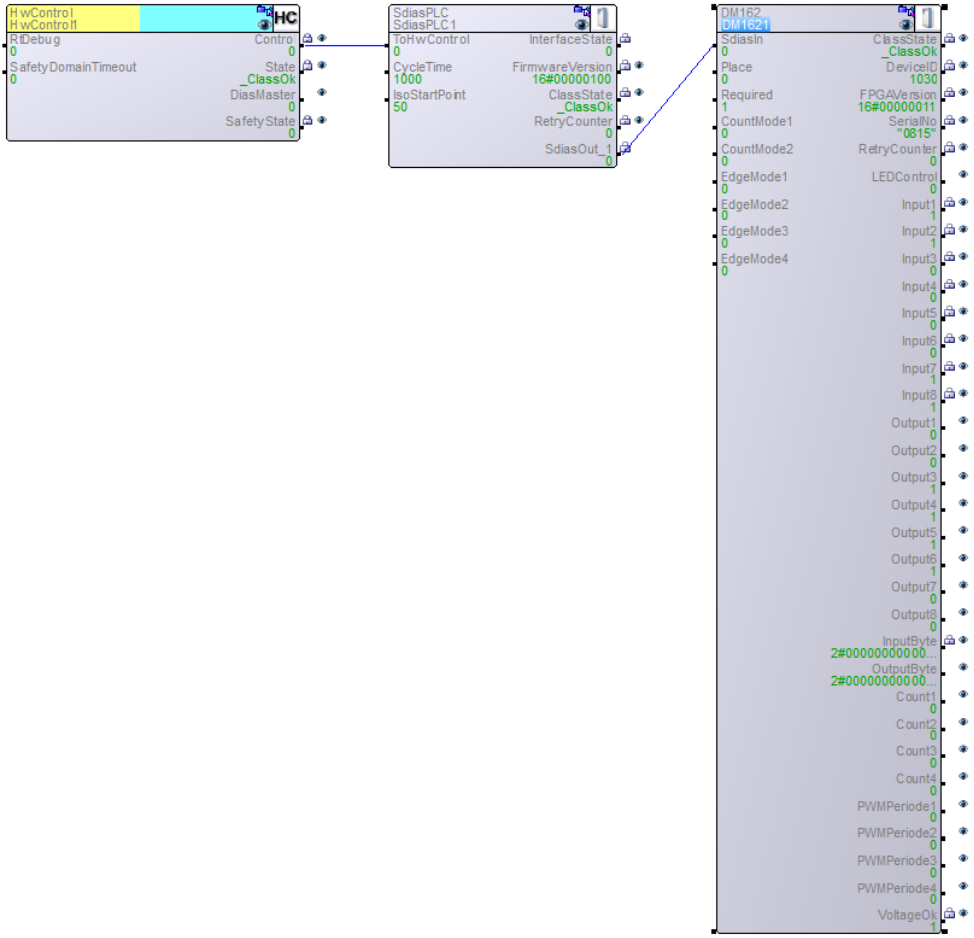
2) If mode register is set for counter mode

3) If mode register is set for incremental encoder mode

4) If mode register is set for time stamp mode

5) If mode register is set for PWM mode

9.4 Example


HwControl
HwControl1
HC
RtDebug
0
SafetyDomainTimeout
0
Control
0
State
_ClassOk
DiasMaster
0
SafetyState
0
SdiasPLC
SdiasPLC1
ToHwControl
0
CycleTime
1000
IsoStartPoint
50
InterfaceState
0
FirmwareVersion
16#00000100
ClassState
_ClassOk
RetryCounter
0
SdiasOut_1
0
DM162
DM1621
SdiasIn
0
Place
0
Required
1
CountMode1
0
CountMode2
0
EdgeMode1
0
EdgeMode2
0
EdgeMode3
0
EdgeMode4
0
ClassState
_ClassOk
DeviceID
1030
FPGAVersion
16#00000011
SerialNo
"0815"
RetryCounter
0
LEDControl
0
Input1
1
Input2
1
Input3
0
Input4
0
Input5
0
Input6
0
Input7
1
Input8
1
Output1
0
Output2
0
Output3
1
Output4
1
Output5
1
Output6
1
Output7
0
Output8
0
InputByte
2#0000000000...
OutputByte
2#0000000000...
Count1
0
Count2
0
Count3
0
Count4
0
PWMPeriode1
0
PWMPeriode2
0
PWMPeriode3
0
PWMPeriode4
0
VoltageOk
1

Documentation Changes

Change date	Affected page(s)	Chapter	Note
01.04.2014	10	5 mounting	Text updated
30.01.2014	9	4.2 Notes	Note regarding connecting/disconnecting the S-DIAS module under voltage.
26.03.2015	7	3.2 Applicable Connectors	Added connections
25.11.2015	11 14	6 Description of the Counters 7 Addressing	added corrected
11.01.2016	11	6 Description of the Counters	Updated chapter
21.01.2016	4	1.5 Miscellaneous	Standard changed
25.01.2016	4	1.3 Electrical Requirements	Graphics added
28.04.2016	13	5 Mounting	Graphics distances
13.06.2016	4	1.3 Electrical Requirements	Current consumption adjusted
27.10.2016	17, 18, 19	6.1.1 Edge Mode with ris. 6.1.2 Edge Mode with fall. 6.1.3 Edge Mode with both.	Diagrams expanded
17.08.2017	7 10	1.6 Environmental Conditions 3.2 Applicable Connectors	Added operating conditions Added sleeve length Added info regarding ultrasonically welded strands
18.10.2017	11 15	3.3 Label Field 5 Mounting	Added chapter Graphic replaced
27.02.2019	17	6.1 Time Stamp Mode	Graphic renewed
26.09.2019	9	3 Connector Layout	Graphics extended, note added
14.11.2019	25	8 Supported Cycle Times	Chapter added
28.02.2020	25	8 Supported Cycle Times	Text adapted
08.09.2020	26	9 Hardware Class DM162	Chapter added
04.11.2020	14	5 Mounting	Expansion functional ground connection
30.08.2021	4	1.1 Digital Input Specifications	Signal level and Switching threshold

23.12.2021	5	1.2 Digital Output Specifications	Delay values changed
03.06.2022	7	1.5 Miscellaneous	HW version